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CMRIT

Internal Assessment Test 4 – Mar 2022

Sub:	Computer Organization and Architecture					Sub Code:	18EC35	Branch:	ECE
Date:	19-03-2022	Duration:	180 Minutes	Max Marks:	100	Sem / Sec:	3/A,B,C,D		OBE

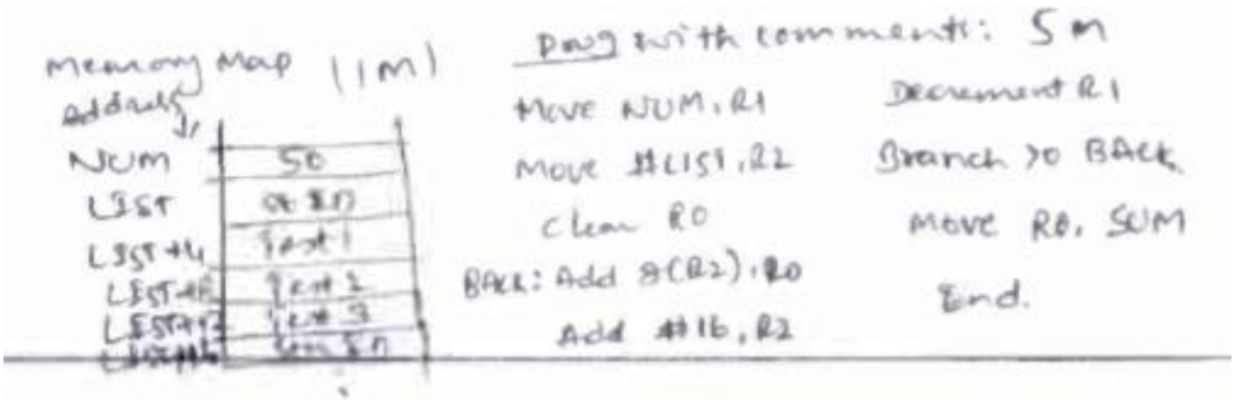
	Answer any FIVE FULL Questions	MARKS	CO	RBT
1	Consider a set of numbers(each 4 bytes in size) stored in memory starting at address TABLE. Total numbers are N and this value is stored at location LOCN. (i) Sketch the memory map showing all details. (ii) Develop an ALP using Auto-increment addressing mode, to compute the sum of all numbers and store the result at memory address RESULT. Write appropriate comments.	[10]	CO2	L3
2	Perform subtraction on the following pairs of numbers using 5-bit signed 2's complement format. Indicate about overflow in each case. (i) +10 and -8 (ii) +12 and +9 (iii) -15 and -9 (iv) -14 and +5	[10]	CO1	L2
3	Consider a register R1 to size 16 bits with initial data 5867d. With neat sketches, depict the output in each case, after performing the following operations: (i) LShiftL #2, R1 (ii) AShiftR #1, R1 (iii) RotateR #1, R1 Note: For each operation, R1 value is to be taken as 5867d and carry flag is indicated cleared.	[10]	CO2	L3
4	Explain single bus organization of datapath in a processor with a neat diagram.	[10]	CO5	L3
5	Explain the basic concepts of computer with neat diagram of connection between memory and processor.	[10]	CO1	L2
6	Write an ALP to add 'n' numbers using Indirect Addressing Mode with appropriate comments.	[10]	CO2	L3
7	Write short note on IEEE format of floating representation with example of 32 bit representation of 1259.125	[10]	CO1	L2
8	With a neat diagram, discuss three bus organization of CPU. Compare the performance with single-bus organization.	[10]	CO5	L2
9	Briefly Discuss types of Computers. Discuss the Functional units of computer with diagram.	[10]	CO1	L2
10	Consider a database of marks scored by students in 3 tests, stored in memory starting at address LIST. Each student record consists of student ID followed by marks in 3 tests. Assume each of these to be 4 bytes in size. There are 50 students in the class and this value is stored at location NUM. (i) Sketch the memory map showing all details. (ii) Develop an ALP using Indexed Addressing mode, to compute the sum of scores by all the students in Test2 and store the result in location SUM. Write appropriate comments.	[10]	CO2	L3
11	Distinguish between Big-endian and Little-endian memory assignment. With a neat sketch, show how the number 26789435 is stored using these methods.	[10]	CO1	L2
12	Explain the organization of a complete processor, with the help of a block diagram.	[10]	CO5	L2
13	What is Subroutine? With a pseudo code or program segment, illustrate parameter passing using registers.	[10]	CO2	L2
14	Discuss Hardwired control unit organization with relevant diagrams and illustrate the logic to generate Z_{in} control signal.	[10]	CO5	L3
15	With a block diagram, describe the organization of a microprogrammed control unit.	[10]	CO5	L3

18EC35-COA IAT2 Scheme and Solution, Jan 2022

1. Consider a database of marks scored by students in 3 tests, stored in memory starting at address LIST. Each student record consists of student ID followed by marks in 3 tests. Assume each of these to be 4 bytes in size. There are 50 students in the class and this value is stored at location NUM. Sketch the memory map showing all details. Develop an ALP using Indexed Addressing mode, to compute the sum of scores by all the students in Test2 and store the result in location SUM. Write appropriate comments.(10)

Memory map-3 M

Program with comments-8 M


Memory Map (1M)
address
NUM 50
LIST St ID
LIST+4 Test 1
LIST+8 Test 2
LIST+12 Test 3
LIST+16 Stu ID

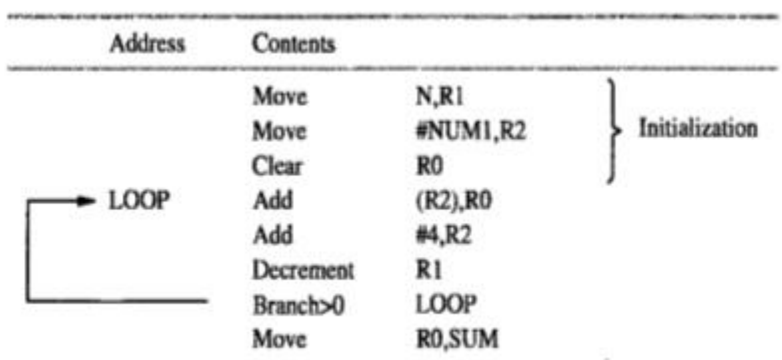
Prog with comments: 5m

```
      Move NUM, R1
      Move #LIST, R2
      Clear R0
BACK: Add 8(R2), R0
      Add #16, R2
      Decrement R1
      Branch>0 BACK
      Move R0, SUM
      End.
```

2. Write an ALP to add 'n' numbers using Indirect Addressing Mode with appropriate comments.

ALP- 5 M

Comments-5 M



Address	Contents		
	Move	N,R1	Initialization
	Move	#NUM1,R2	
	Clear	R0	
LOOP	Add	(R2),R0	
	Add	#4,R2	
	Decrement	R1	
	Branch>0	LOOP	
	Move	R0,SUM	

Figure 2.12 Use of indirect addressing in the program of Figure 2.10.

3. Illustrate DMA with registers involved in its interface.

Diagram and Registers-5 M

Explanation-5 M

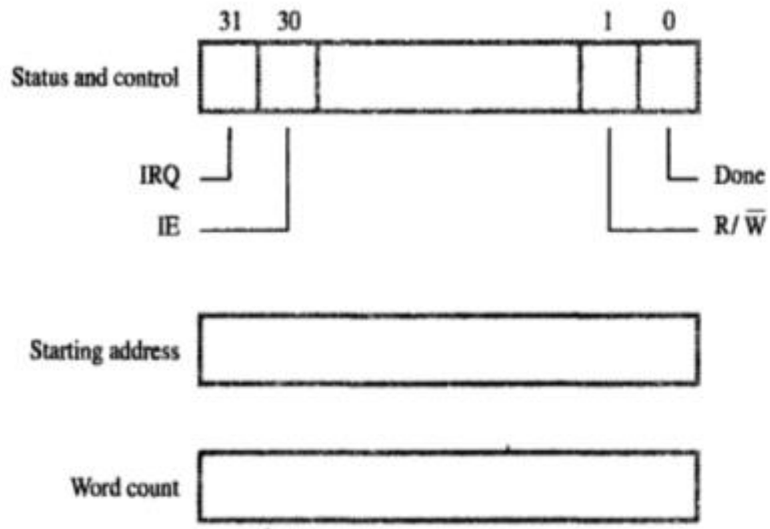


Figure 4.18 Registers in a DMA interface.

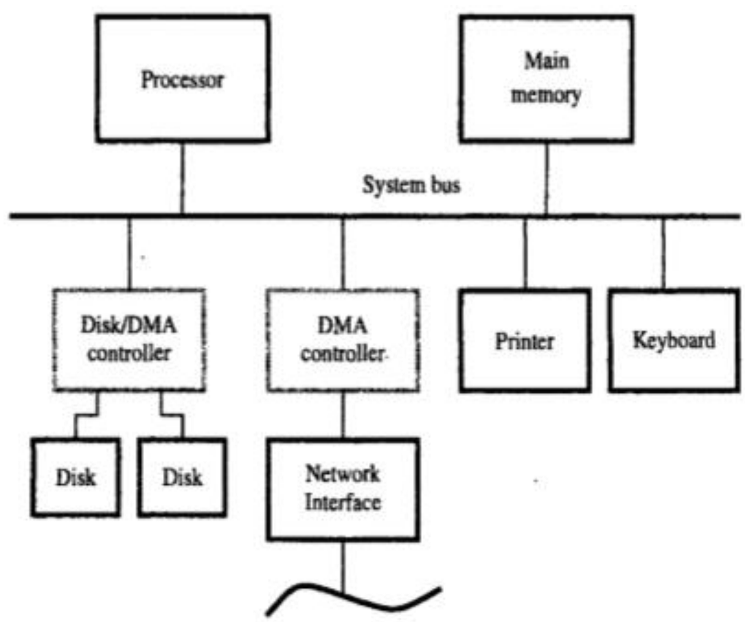


Figure 4.19 Use of DMA controllers in a computer system.

4. Consider a register R1 to size 16 bits with initial data 5867d. With neat sketches, depict the output in each case, after performing the following operations: (i)LShiftL #2, R1 (ii) AShiftR #1, R1 (iii) RotateR #1, R1 Note: For each operation, R1 value is to be taken as 5867d and carry flag is indicated cleared.

First convert the given decimal to binary. 1 M

With neat sketches, demonstrate the shifts and rotations. 9 M(3 marks each)

5. With a neat diagram, discuss implementation of interrupt priority using individual request and acknowledgement lines.

Diagram-3 M

Explanation-7 M

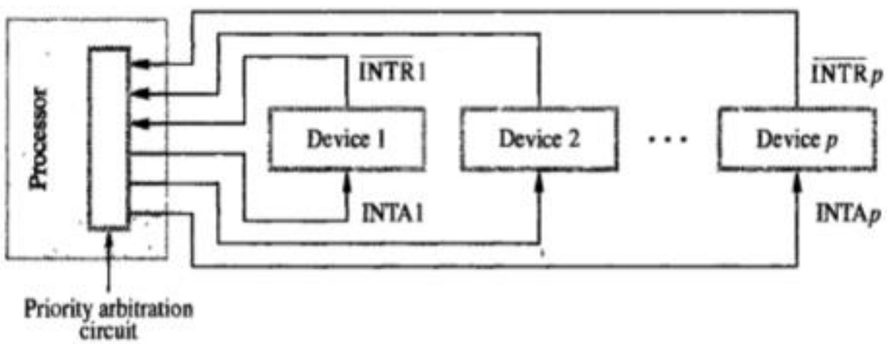


Figure 4.7 Implementation of interrupt priority using individual interrupt-request and acknowledge lines.

6. What is an Interrupt? With an example, illustrate the concept of interrupt.

DIagram-2 M

Explanation-8 M

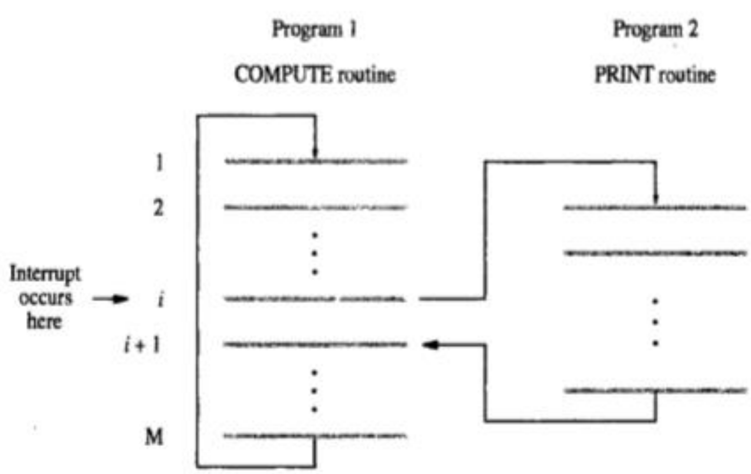


Figure 4.5 Transfer of control through the use of interrupts.

7.a. What is Subroutine? With a pseudocode or program segment, illustrate parameter passing using registers.

Code- 5 M

Explanation-5 M

Calling program

```
        Move     N, R1              R1 serves as a counter
        Move     #NUM1, R2          R2 points to the list
        Call     LISTADD            Call subroutine
        Move     R0, SUM            Save result
                 •
                 •
                 •
```

Subroutine

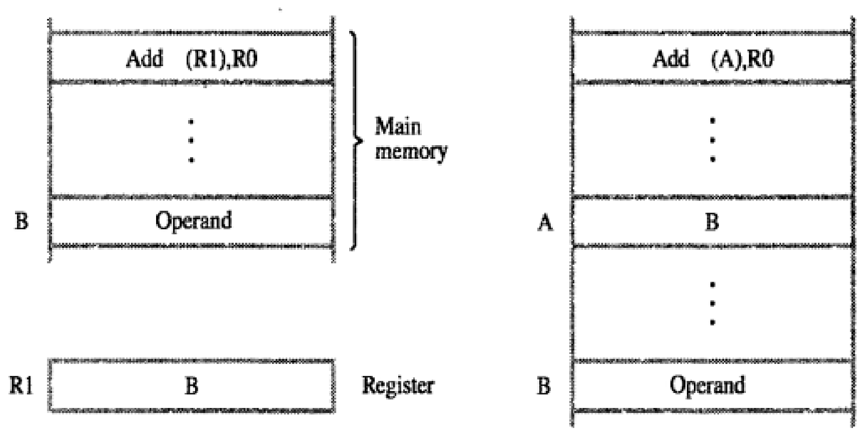
```
LISTADD   Clear      R0             Initialize sum to 0

LOOP      Add        (R2)+, R0      Add entry from list
          Decrement  R1
          Branch > 0 LOOP
          Return                    Return to calling program
```

Fig 2.7: Program written as a subroutine; parameters passed through registers

7. b. Explain Indirect and Indexed Addressing Modes with suitable examples.

Example code for each-5 M

Explanation- 5 M



a) Through a general purpose register b) Through a memory location

Fig 2.1: Indirect addressing

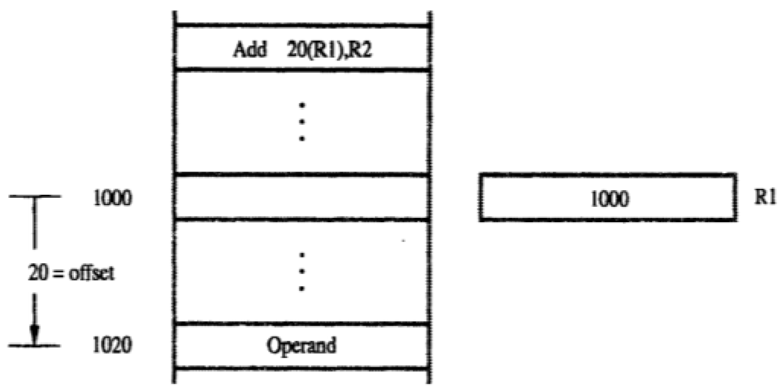


Fig 2.2 a: Offset is given as a constant

8. Consider a set of numbers(each 4 bytes in size) stored in memory starting at address TABLE. Total numbers are N and this value is stored at location LOCN. Sketch the memory map showing all details. Develop an ALP using Auto-increment addressing mode, to compute the sum of all numbers and store the result at memory address RESULT. Write appropriate comments.

Code-5 M

Explanation/comments-5 M

Auto-increment & Auto-decrement A.M. 2M

mem. map (1M) prog. with comments (5M)


```
      Move LOCN, R1
      Move #TABLE, R2
      Clear R0
UP:   Add (R2)+, R0
      Decrement R1
      Branch>0 UP
      Move R0, RESULT
      End
```

COA IAT3 Scheme and Solution Feb 2022

1. Explain single bus organization of datapath in a processor with a neat diagram. (10)

Diagram-5 M

Explanation on each block-5 M

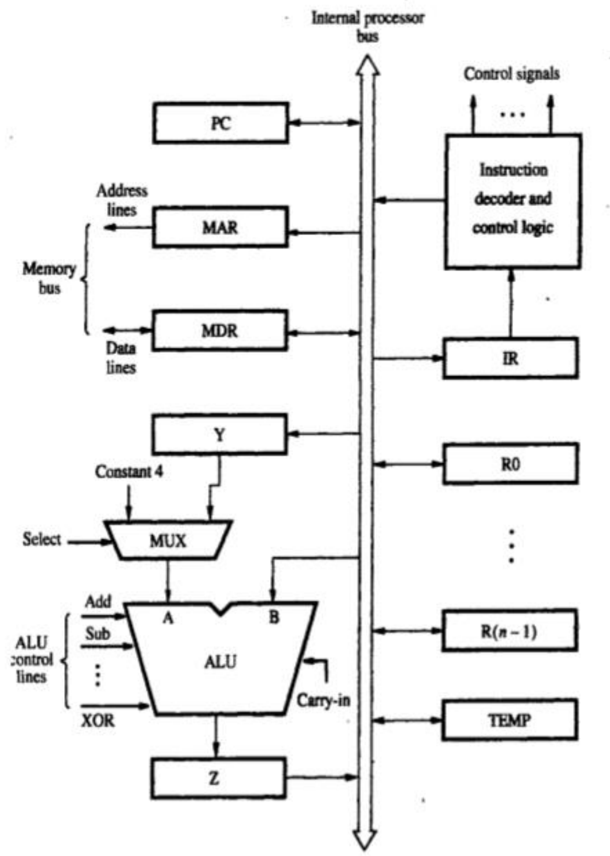


Figure 7.1 Single-bus organization of the datapath inside a processor.

2. Describe the sequence of control signals to be generated to fetch an instruction from memory in a single bus organization.

Sequence-5 M

Explanation-5 M

Step	Action
1	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}
2	Z_{out}, PC_{in}, Y_{in}, WMFC
3	MDR_{out}, IR_{in}
4	$R3_{out}$, MAR_{in}, Read
5	$R1_{out}$, Y_{in}, WMFC
6	MDR_{out}, SelectY, Add, Z_{in}
7	Z_{out}, $R1_{in}$, End

Figure 7.6 Control sequence for execution of the instruction Add (R3),R1.

3. Explain the organization of a complete processor, with the help of a block

Diagram.

Diagram-5 M

Explanation-5 M

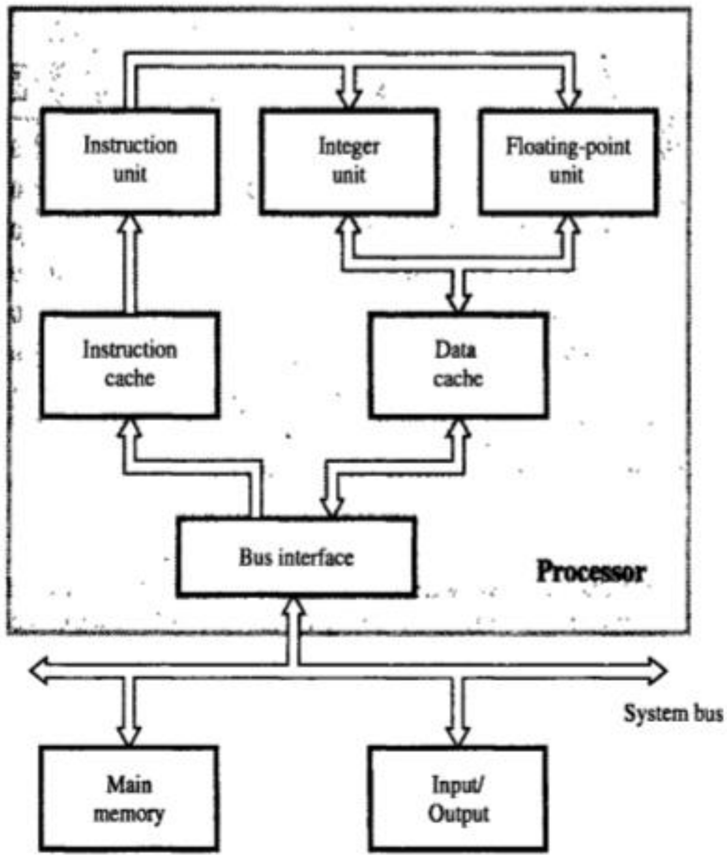


Figure 7.14 Block diagram of a complete processor.

4. With a neat diagram, discuss three bus organization of CPU. Compare the performance with single-bus organization.

Diagram-5 M

Explanation-5 M

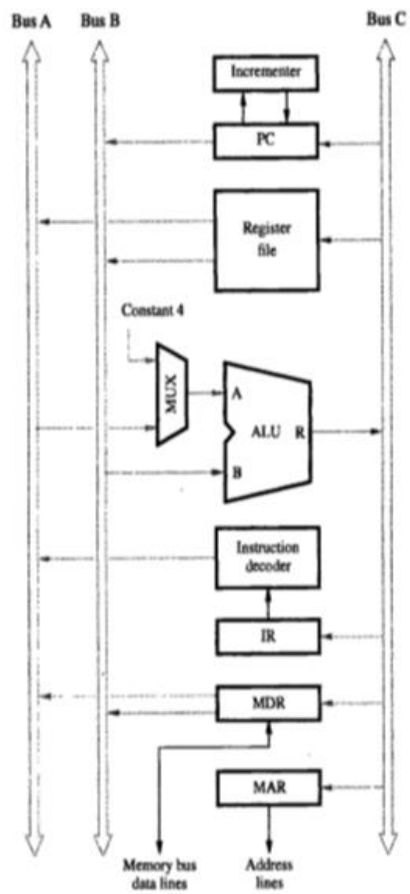


Figure 7.8 Three-bus organization of the datapath.

5. Discuss Hardwired control unit organization with relevant diagrams and illustrate the logic to generate Z in control signal.

Diagrams- 5 M

Explanation- 5 M

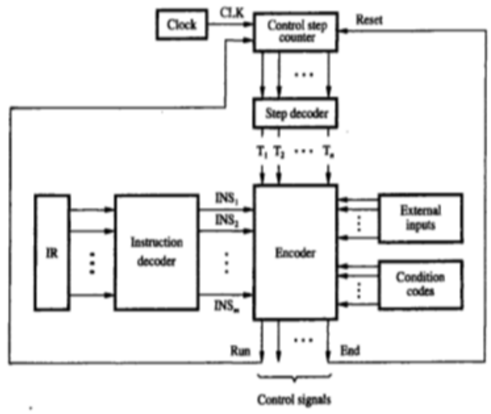


Figure 7.11 Separation of the decoding and encoding functions.

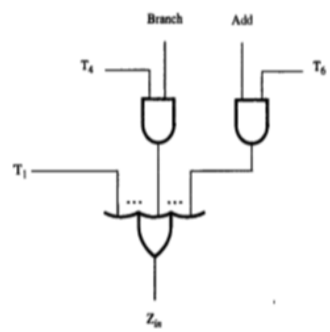


Figure 7.12 Generation of the Z_{in} control signal for the processor in Figure 7.1.

6. Write a microroutine for any conditional branching instruction(with suitable comments) w.r.t Microprogrammed control.

Microroutine-5 M

Explanation-5 M

Address	Microinstruction
0	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}
1	Z_{out}, PC_{in}, Y_{in}, WMFC
2	MDR_{out}, IR_{in}
3	Branch to starting address of appropriate microroutine
...	...
25	If N=0, then branch to microinstruction 0
26	Offset-field-of-IR_{out}, SelectY, Add, Z_{in}
27	Z_{out}, PC_{in}, End

Figure 7.17 Microroutine for the instruction Branch < 0.

7. With a block diagram, describe the organization of a microprogrammed control unit.

Diagram-5 M

Explanation-5 M

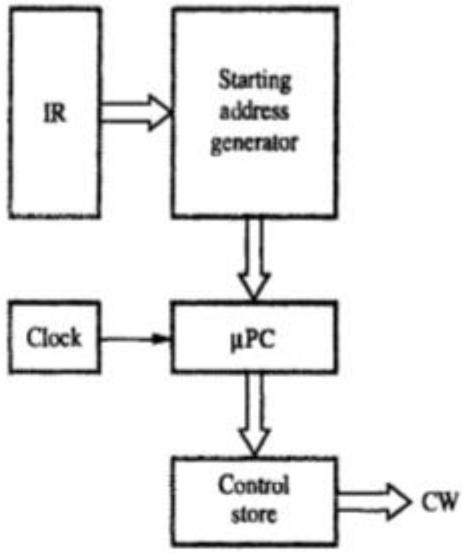


Figure 7.16 Basic organization of a microprogrammed control unit.