Seventh Semester B.E. Degree Examination, July/August 2022
Embedded Computing Systems

Time: 3 hrs.　　　　　　　　　　　　　　　　　　　　　　　　　Max. Marks:100

Note: *Answer any FIVE full questions, selecting at least TWO full questions from each part.*

PART – A

1　a.　With neat figure explain the design process involved in an embedded system design.
　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　(08 Marks)
　b.　List and explain the requirement chart for the GPS moving map.　　**(04 Marks)**
　c.　With neat UML diagram, explain signal, call and time out events.　　**(08 Marks)**

2　a.　Draw two different types of computer architectures and list the differences between them.
　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　(08 Marks)
　b.　Write the ARM assembly code for $x = (a + b) - c$;　　　　　　　**(04 Marks)**
　c.　With neat diagrams, explain the following:
　　　i)　　Direct mapped cache　　　ii) Sect Associative cache.　　**(08 Marks)**

3　a.　Briefly explain the major components of a bus protocol. With neat diagram, explain burst read transaction.　　　　　　　　　　　　　　　　　　　　**(08 Marks)**
　b.　With neat figure, explain the hardware architecture of a PC.　　　**(08 Marks)**
　c.　Define DMA controller and explain its functionalities.　　　　　　**(04 Marks)**

4　a.　With neat figure explain circular buffer for streaming data in Embedded systems.　**(04 Marks)**
　b.　Briefly explain different types of optimization techniques.　　　　**(08 Marks)**
　c.　Write about　i) Clear-Box Testing　　ii) Black-Box Testing.　　**(08 Marks)**

PART – B

5　a.　Define RTOS. With neat figure, explain the different RTOS Kernel services.　**(08 Marks)**
　b.　Distinguish between process and threads.　　　　　　　　　　　**(06 Marks)**
　c.　Explain various queues involved in task scheduling with a neat diagram.　**(06 Marks)**

6　a.　Explain the working procedure of memory mapped objects.　　　　**(06 Marks)**
　b.　Define RPC. Explain its operation with a neat diagram.　　　　　**(06 Marks)**
　c.　Three processes with process IDs P_1, P_2, P_3 with estimated completion time 10, 5, 7 milliseconds respectively. Calculate the waiting time and Turn Around Time (TAT) for each process and the average waiting time and average Turn Around Time. If a new process P_4 with estimated time 2ms enters the ready queue after 2ms of execution of P_2 in SJF algorithm (non-preemptive). Assume all the processes contain only CPU operations and no I/O operations are involved.　　　　　　　　　　　　　　　　　　**(08 Marks)**

7　a.　With neat diagram, explain I^2C Bus and its operations.　　　　　**(06 Marks)**
　b.　Briefly explain the functionalities of Ethernet CSMA/CD algorithm.　**(04 Marks)**
　c.　Define Multihop communication with a neat figure.　　　　　　　**(04 Marks)**
　d.　Explain the data frame format of a CAN.　　　　　　　　　　　**(06 Marks)**

8　a.　Briefly explain the following:
　　　i)　　Simulator with its advantages and limitations.
　　　ii)　　In-circuit Emulator.　　　　　　　　　　　　　　　　**(12 Marks)**
　b.　Explain the various hardware debugging tools used in Embedded Product development.
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