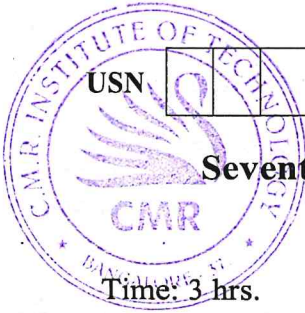# CBCS SCHEME

17CS72

Seventh Semester B.E. Degree Examination, July/August 2022
Advanced Computer Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain different shared memory multiprocessor models. **(08 Marks)**
   b. Explain PRAM model. **(06 Marks)**
   c. What are different static interconnection networks? Explain any two networks. **(06 Marks)**

OR

2 a. Explain the Bernstein's conditions for parallelism. For the program statements given draw the dependence graph.
   S1: $A = B + D$, S2: $C = A \times 3$, S3: $A = A + C$, S4; $E = A/2$. **(10 Marks)**
   b. Explain Amdahl's law. In a multi-processor system with 9 processors, the portion for parallel programming is 75% then calculate overall speedup. If number of processors is doubled and with same program conditions what is the new speed up. Use Amdahl's law to calculate the speed-up. **(10 Marks)**

Module-2

3 a. Explain with diagram general CISC and RISC architectures. **(10 Marks)**
   b. Explain VLIW architecture with its instruction pipelining. **(10 Marks)**

OR

4 a. Explain different virtual memory models. **(10 Marks)**
   b. What are different page-replacement policies? A certain program generates following page trace.
   Page trace: 0 1 2 4 2 3 7 2 1 3 1
   These pages are to be mapped on to three page frames (PFs). Use LRU algorithm and show the pages residing in the page frames. Calculate the hit ratio. **(10 Marks)**

Module-3

5 a. With a diagram, explain backplane bus system. **(10 Marks)**
   b. Explain sequential and weak consistency memory models. **(10 Marks)**

OR

6 a. Explain with diagram the asynchronous and synchronous models of linear pipeline processors. **(08 Marks)**
   b. Explain arithmetic pipeline stages with an adder unit. **(06 Marks)**
   c. What are different branch prediction methods? Explain briefly. **(06 Marks)**

Module-4

7   a.   Explain cross bar network and cross-point switch design in a multiprocessor system.

(06 Marks)

   b.   What is cache coherence problem in data sharing? Explain different causes for that.

(08 Marks)

   c.   What are different vector access memory schemes? Explain any one.   (06 Marks)

OR

8   a.   What are the different latency hiding techniques? Explain two of them.   (10 Marks)

   b.   Explain static, dynamic and pure dataflow machines.   (10 Marks)

Module-5

9   a.   What are different programming models? Explain message-passing model.   (08 Marks)

   b.   Explain the compilation phases in parallel computing environment with a diagram. (06 Marks)

   c.   Explain testing algorithm with dependence test.   (06 Marks)

OR

10 a.   What are the different synchronization schemes in multiprocessor system? Explain any two of them.   (10 Marks)

   b.   Explain the following terms in parallel architecture:
     i)   Operand Forwarding
     ii)   Reorder buffer.   (10 Marks)

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