CBCS SCHEME

USN | | | | | | | | | | |

18EC72

Seventh Semester B.E. Degree Examination, July/August 2022
VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Derive the expression for drain current in linear and saturation region for nmos transistor. **(10 Marks)**

b. Implement the following circuits using CMOS logic
i) Inverter
ii) Pass transistor. **(10 Marks)**

OR

2 a. Explain the non ideal IV effect of MOSFET with respect to CMOS Channel length modulation and also explain Noise Margin with diagram and equations. **(10 Marks)**

b. Implements the following circuits using CMOS logic
i) 2 input NAND gate
ii) Transmission gate. **10 Marks)**

Module-2

3 a. Describe with neat sketches the fabrication of P – well CMOS inverter. **(08 Marks)**

b. Explain the process of photolithography with a neat diagram in CMOS technologies. **(06 Marks)**

c. Draw the stick diagram for the following CMOS logic
i) $Y = \overline{A + B + C}$
ii) 2 input NAND gate. **(06 Marks)**

OR

4 a. Explain the layout Design Rules for MOS process with two metal layers. **(06 Marks)**

b. Draw the stick diagram for the CMOS logic $Y = \overline{(A + B + C)D}$ and estimate the cell area. **(06 Marks)**

c. Define scaling. Explain the constant voltage scaling and the effect of scaling on device characteristics. **(08 Marks)**

Module-3

5 a. Explain with a waveform the propagation Delay, Rise times and Fall Times of a CMOS inverter. **(08 Marks)**

b. Derive the equation of propagation Delay using RC Delay Model for a 1st order system. **(06 Marks)**

c. Compute the Elmore Delay for V_{out} in the 2nd order RC system. **(06 Marks)**

OR

6 a. Explain Parasitic Delay of common gates in Linear Delay Model. **(08 Marks)**

b. Design a circuit to compute F = AB + CD using NAND and NOR by Bubble pushing. **(06 Marks)**

c. Calculate the minimum delay in C to compute F = AB + CD using the circuits with NAND and NOR gates and with AOI gates. Each input can present a maximum of 20λ of transistor width. The output must derive a load equivalent to 100λ of transistor width. Choose transistor sizes to achieve this delay. **(06 Marks)**

Module-4

7 a. Explain Resettable Latches and FlipFlops using CMOs transmission Gate. **(10 Marks)**

b. Explain the Multistage pass transistor logic driven by two non overlapping clocks. **(10 Marks)**

OR

8 a. Explain conventional CMOs flipflops with neat diagrams. **(10 Marks)**

b. Explain Domino CMOS Logic. **(10 Marks)**

Module-5

9 a. Explain the operation of three transistor dynamic RAM cell. **(10 Marks)**

b. Explain Full CMOS static RAM cell with schematic diagram. **(10 Marks)**

OR

10 a. Write short notes on :

i) Built in Self Test (BIST)

ii) Scan Design Technology **(10 Marks)**

b. Explain briefly logic verification principle with a block diagram. **(10 Marks)**

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