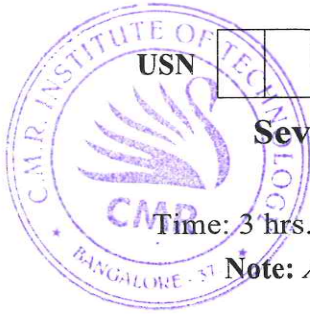


CBCS SCHEME

15TE73



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Seventh Semester B.E. Degree Examination, July/August 2022 CMOS VLSI Design

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Discuss the working of nMOS enhancement mode transistor operation with neat diagrams. (06 Marks)
- b. Explain the CMOS inverter DC characteristics highlighting the regions of operation. (10 Marks)

OR

- 2 a. Explain body effect as non ideal I-V effect of MOSFET. (03 Marks)
- b. Explain Noise margin, with respect to CMOS inverter. (05 Marks)
- c. Explain the steps of nMOS fabrication with neat diagrams. (08 Marks)

Module-2

- 3 a. Discuss CMOS design styles with neat diagrams. (05 Marks)
- b. Draw the stick diagram for the following using CMOS logic
 - i) $Y = \overline{A + BC}$
 - ii) $(A + B) \cdot C = Y$(05 Marks)
- c. Discuss the different contact cuts with an example to each. (06 Marks)

OR

- 4 a. With a neat diagram, derive an expression for sheet resistance and mention the R_s values of metal, P and n transistor for $5\mu\text{m}$ technology. (05 Marks)
- b. Derive an equation for rise time and fall time with respect to CMOS Inverter. (08 Marks)
- c. Draw the circuit and stick diagram for 2i/p NOR gate using CMOS Logic. (03 Marks)

Module-3

- 5 a. Explain the constant field, constant voltage scaling models with a diagram and scaling effect table. (06 Marks)
- b. Discuss the three different bus architectures. (06 Marks)
- c. Discuss the problems associated in VLSI design. How do you reduce them? (04 Marks)

OR

- 6 a. Discuss the design of 4 bit Adder. (07 Marks)
- b. With relevant diagrams, discuss Manchester carry chain operation. (05 Marks)
- c. Explain the carry select adder with a diagram. (04 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-4

- 7 a. Discuss programmable logic array with its block diagram, general architecture and floor plan. (08 Marks)
b. Discuss the architectural issue related to VLSI subsystem design. (08 Marks)

OR

- 8 a. Explain the architecture of field programmable gate array. (08 Marks)
b. Discuss the FPGA abstractions with diagrams. (08 Marks)

Module-5

- 9 a. Explain three transistors DRAM with its circuit diagram and stick diagram. (07 Marks)
b. Discuss the ASM chart for JKFF with its NAND logic arrangement. (09 Marks)

OR

- 10 a. Explain logic verification process with its functional equivalent diagram. (06 Marks)
b. Discuss the design for manufacturability. (06 Marks)
c. Discuss the Ad-hoc testing. (04 Marks)

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