CBCS SCHEME

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18EC56

Fifth Semester B.E. Degree Examination, July/August 2022
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With neat block diagram of 4-bit Ripple carry counter. Explain the design hierarchy. **(10 Marks)**

b. Explain typical design flow for designing VLSI circuit, using the flow chart diagram. **(10 Marks)**

OR

2 a. What are the two styles of stimulus application? Explain each method in brief. **(08 Marks)**

b. Explain the following terms with examples : (i) module (ii) instances **(06 Marks)**

c. What are the advantages of verilog HDL? List out importance of HDL's. **(06 Marks)**

Module-2

3 a. What is ports? Explain the two methods of connecting Ports to external signals with examples. **(06 Marks)**

b. Explain the following data types with an example in verilog:
(i) Nets (ii) Register (iii) Vectors (iv) Parameters **(08 Marks)**

c. What are the basic components of module? Explain all components of verilog module. **(06 Marks)**

OR

4 a. What are the four values and eight strengths support in verilog HDL? List out in neat table. **(06 Marks)**

b. With example explain different types of lexical conventions. **(08 Marks)**

c. Declare following variables in verilog :
(i) Decimal number 123 as a sized 8 bit number in binary. Use for readability.
(ii) A 16-bit hexadecimal unknown number with all X's.
(iii) A 4-bit negative 2 in decimal. Write the 2's complement form for this number.
(iv) An unsized hex number 1234. **(06 Marks)**

Module-3

5 a. Write a verilog data flow description for 4-bit full adder with carry look ahead. **(10 Marks)**

b. What would be the output of the following:
a = 4'b1010 , b = 4'b1111
(i) a&b (ii) a&&b (iii) &a (iv) a>>1 (v) a>>>1
(vi) $y = \{2\{a\}\}$ (vii) $a \wedge b$ (viii) $z = \{a, b\}$ **(10 Marks)**

OR

6 a. Discuss AND/OR and NOT gates with respect to logic symbols, gate installation and truth table. **(10 Marks)**

b. Define butif/notif and write gate installation of bufit, notif gates. **(10 Marks)**

Module-4

7 a. Explain the blocking assignment statements and non blocking assignment statements with relevant examples. **(06 Marks)**

b. Write a verilog program for 8 : 1 mux using case statement and test bends. **(08 Marks)**

c. Using forever statement, design a clock with period time = 10 and duty cycle = 40%, initial value of clock is 0. **(06 Marks)**

OR

8 a. Explain sequential and parallel blocks with examples. **(06 Marks)**

b. Write the verilog behavioural description of a 4 bit binary counter with test cases. **(08 Marks)**

c. Using the for loop, initialize locations 0 to 1023 of a 4 bit register array cache_Var to 0. **(06 Marks)**

Module-5

9 a. Explain the synthesis flow for 4 bit magnitude comparator. **(10 Marks)**

b. Write a note on verification of gate-level netlist. **(10 Marks)**

OR

10 a. Write a note on : (i) Force and release (ii) defparam statement (iii) time scale (iv) file output **(10 Marks)**

b. Define the term logic synthesis with neat flow chart, explain computer Aided logic synthesis process. **(10 Marks)**

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