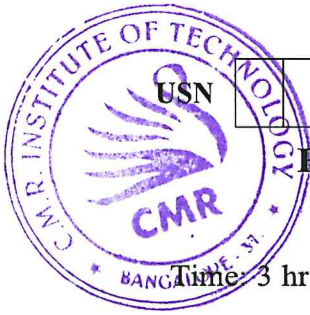


CBCS SCHEME



15EC53

Fifth Semester B.E. Degree Examination, July/August 2022

Verilog HDL

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain the typical design flow for designing VLSI IC circuits, with a neat flow chart. (08 Marks)
- b. Explain Bottom – up design Methodology, with an example. (08 Marks)

OR

- 2 a. Explain Stimulus block with an example. (08 Marks)
- b. Explain with example different levels of abstraction used in Verilog programming. (08 Marks)

Module-2

- 3 a. List and explain Basic Lexical Conventions used by Verilog HDL. (08 Marks)
- b. Explain System tasks, with an example each. (08 Marks)

OR

- 4 a. Explain Verilog Ports and Port Connection rules. (08 Marks)
- b. What are the basic components of a Module? Explain it with a block diagram and an example which components are mandatory. (08 Marks)

Module-3

- 5 a. Write the Truth tables for AND, OR, NAND, NOR, XOR, XNOR gates when inputs to the gates take the values {0, 1, X, Z}. (06 Marks)
- b. Write a verilog code for 4 – to – 1 Multiplexer using gate level descriptive style and the logic diagram for 4 : 1 Mix. Illustrate its working using stimulus block. (10 Marks)

OR

- 6 a. Define i) Shift operators ii) Reduction operators iii) Equality operators with an example each. (06 Marks)
- b. Write the Data flow descriptive style of verilog code for 4 – bit magnitude comparator, which takes the input $A = A(3) A(2) A(1) A(0)$ and $B = B(3) B(2) B(1) B(0)$ where Left – most bit is the most significant bit. (10 Marks)

Module-4

- 7 a. Explain the structured procedures “always” and “initial” block in behavioral modeling with examples. (08 Marks)
- b. Explain Delay – based timing control mechanism in behavioural modeling with examples for each category. (08 Marks)

OR

- 8 a. Explain Multiway Branching using “Case”, “CaseX” and “CaseZ” statements. (08 Marks)
- b. Describe Event based timing control mechanism in behavioural modeling with examples for each category. (08 Marks)

Module-5

- 9 a. Explain the declaration of constant , variable and signal in VHDL with example. (08 Marks)
b. Write a VHDL program for Half Subtractor using behavioral description. (08 Marks)

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- 10 a. Explain Synthesis process in VHDL with an example. (08 Marks)
b. Write a VHDL code for full adder using 2 half address. Use Structural descriptive style. (08 Marks)
