USN | | | | | | | | | | **20EVE241**
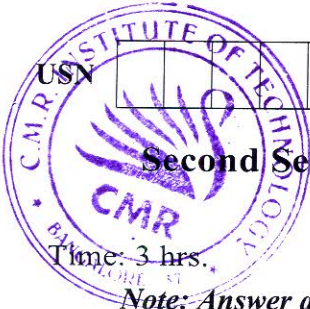
Second Semester M.Tech. Degree Examination, Feb./Mar. 2022
Advances in VLSI Design

Time: 3 hrs.   Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1. a. Explain standard cell based design techniques. **(10 Marks)**
   b. Explain semi-custom design flow. **(10 Marks)**

OR

2. a. Explain Pre-diffused (or mask-programmable) arrays. **(10 Marks)**
   b. With a neat diagram, Explain switch-box based programmable interconnect. **(10 Marks)**

Module-2

3. a. Explain briefly interwire capacitance and cross-talk. **(08 Marks)**
   b. Explain about resistance and reliability ohmic voltage drop in resistive parasities. **(08 Marks)**
   c. Explain briefly Electromigration. **(04 Marks)**

OR

4. a. Briefly discuss about the design techniques available to the designer to address the $L\left(\dfrac{di}{dt}\right)$ problem **(12 Marks)**
   b. Explain current mode transmission techniques. **(08 Marks)**

Module-3

5. a. With neat diagrams, differentiate between synchronous and mesochronous interconnect methodologies. **(10 Marks)**
   b. Explain clock skew and clock filter in detail. **(10 Marks)**

OR

6. a. Explain in detail various clock distribution techniques. **(10 Marks)**
   b. With a neat diagram, explain the concept of synchronizer. **(10 Marks)**

Module-4

7. a. Explain general memory architecture and building blocks. **(10 Marks)**
   b. Explain in detail the operation of SRAM cell. **(10 Marks)**

OR

8. a. What is an address decoder? Explain a NAND decoder using 2-input pre-decoder. **(10 Marks)**
   b. Explain the concept of voltage down converters. **(10 Marks)**

Module-5

9. a. Write short notes on: i) Signal to noise ratio   ii) Memory yield. **(10 Marks)**
   b. How is retention current reduced in SRAMS? **(10 Marks)**

OR

10. a. What are the sources of power dissipation in memories? **(10 Marks)**
    b. Explain folded bit-line architecture of IT-DRAM. **(10 Marks)**

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