CBCS SCHEME

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20EVE251

Second Semester M.Tech. Degree Examination, Feb./Mar. 2022
Low Power VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Discuss the need of low power VLSI design. **(05 Marks)**

b. Explain Monte Carlo – simulation technique. **(08 Marks)**

c. Briefly discuss Gate – level logic simulation approach. **(07 Marks)**

OR

2 a. How do you analyse the data correlation in DSP systems? What are the effects of data correlation on bit switching frequency? **(10 Marks)**

b. Discuss architectural level power analysis method. **(10 Marks)**

Module-2

3 a. Define static probability. Derive the equation that relates the static probability 'P' of memoryless random logic signal to its expected frequency f. **(10 Marks)**

b. Define signal entropy. Explain power estimation of combinational logic using entropy analysis. **(10 Marks)**

OR

4 a. Explain various implementations of latches and flip-flop with circuit diagram. **(10 Marks)**

b. Compute the transition density and static probability of y = ab + c. Given P(a) = 0.2, P(b) = 0.3, P(c) = 0.4, D(a) = 1, D(b) = 2, and D(c) = 3. **(10 Marks)**

Module-3

5 a. What is Gate Reorganization? Briefly explain different power saving techniques through gate reorganization, signal gating. **(10 Marks)**

b. Explain Bus invert encoding to achieve low power consumption with relevant equations. **(10 Marks)**

OR

6 a. Explain pre-computation logic with neat block diagram. Also explain binary comparator function using pre-computation logic. **(10 Marks)**

b. Differentiate between single driver scheme and distributed scheme. Explain the concept of buffer insertion in clock tree. **(10 Marks)**

Module-4

7 a. Discuss different types of switching activity reduction with respect to low power VLSI design. **(10 Marks)**

b. With a neat diagram, explain the working of a 8 – bit Wallace tree multiplier. **(10 Marks)**

OR

8 a. Explain flow graph transformation, with operator reduction and control data flow graph and its mapping to hardware architecture. **(10 Marks)**

b. Explain NORA CMOS logic full adder circuit with neat circuit diagram. **(10 Marks)**

Module-5

9 a. Discuss sources and reduction of power dissipation in memory subsystem. **(10 Marks)**

b. For low power CAD framework, explain the design flow with supporting tools. **(10 Marks)**

OR

10 a. Explain the four phases of operations in a four phase adiabatic logic inverter. **(10 Marks)**

b. Discuss state–of–the–art architectural estimation techniques and possible power optimization during synthesis targeted for ASIC architecture style. **(10 Marks)**

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