CBCS SCHEME

USN | | | | | | | | | | |

20EVE12

First Semester M.Tech. Degree Examination, Feb./Mar. 2022
ASIC Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. With neat flow diagram, explain the steps involved in ASIC design. **(10 Marks)**

b. With neat sketches, explain the following :
i) Programmable logic devices
ii) Structured gate arrays. **(10 Marks)**

OR

2 a. With relevant diagram and equations, explain the Conventional Ripple Carry Adder. Mention its limitations. **(10 Marks)**

b. Write a short note on :
i) I/O cells
ii) Cell compilers. **(10 Marks)**

Module-2

3 a. Find the logical effort and logical area of the circuit shown in Fig.Q3(a).

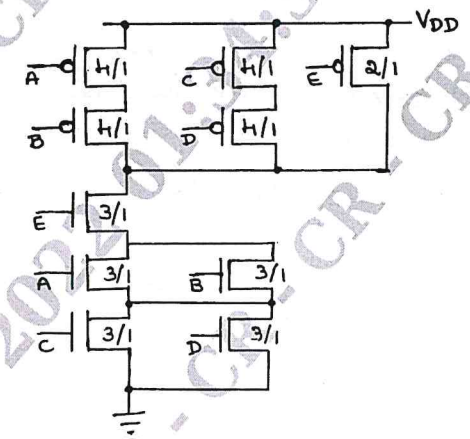

Fig.Q3(a) **(10 Marks)**

b. With neat block diagram explain Altera I/O Block. **(10 Marks)**

OR

4 a. Derive an expression for optimum path delay. **(10 Marks)**

b. Explain Actel Act architecture and Shannon's expansion theorem. **(10 Marks)**

Module-3

5 a. Explain the following :
i) Netlist screeners and its errors
ii) Schematic icons and symbols. **(10 Marks)**

b. With suitable example, explain Kernighan – Lin Algorithm. **(10 Marks)**

OR

6 a. With schematic example, explain the hierarchical design. (10 Marks)
b. Describe the goals and objectives of each steps in ASIC physical design. (05 Marks)
c. Briefly explain the steps involved in constructive partitioning. (05 Marks)

Module-4

7 a. Explain the measurement of delay in floor planning. (10 Marks)
b. Explain the following :
i) Power distribution scheme
ii) Clock planning. (10 Marks)

OR

8 a. Explain physical design flow with respect to placement. (10 Marks)
b. Briefly explain the following :
i) Goals and objectives of placement
ii) Timing driven placement method. (10 Marks)

Module-5

9 a. Explain the following :
i) Left edge algorithm
ii) Hightower area routing algorithm. (10 Marks)
b. Explain circuit extraction and DRC. (10 Marks)

OR

10 a. Explain the following special routing techniques :
i) Clock routing
ii) Power routing. (10 Marks)
b. Explain global routing between blocks. (10 Marks)

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