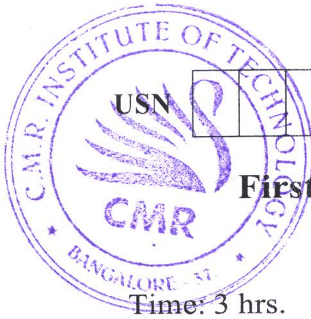

CBCS SCHEME

USN

20EVE14

First Semester M.Tech. Degree Examination, Feb./Mar. 2022
VLSI Testing

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Differentiate between fault and failure with an example. Explain the major fault models used in modern VLSI testing. **(10 Marks)**

b. What is a temporary fault? Explain how temporary faults can be modeled for testing VLSI circuits. **(10 Marks)**

OR

2 a. Explain with examples the types of logic simulation used in VLSI testing **(10 Marks)**

b. What are the delay models used in VLSI testing? Explain with an example for each. **(07 Marks)**

c. Explain stuck–at–faults for a 2-input NAND gate. **(03 Marks)**

Module-2

3 a. List the rules for finding Boolean difference. **(04 Marks)**

b. Explain how Boolean difference can be used in VLSI testing. **(06 Marks)**

c. Find the Boolean difference with respect to x_1 and x_2 in the logic circuit shown in Fig.Q3(c), and give the test patterns for testing for :
i) x_1 s-a-1 and ii) x_2 s-a-0.

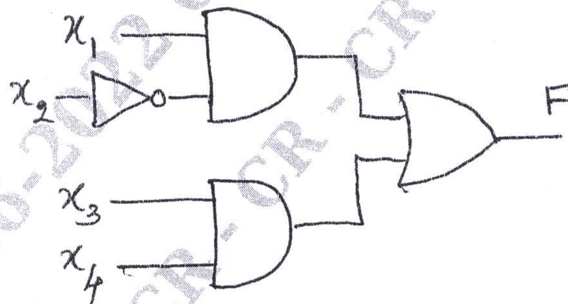

Fig.Q3(c) **(10 Marks)**

OR

4 a. Explain the process of automatic synthesis of testable logic with reference to VLSI circuit design. Elaborate the following with reference to automatic synthesis of testable logic.
i) Translation and optimization phases
ii) Minimization and Restructuring
iii) Cube and Support
iv) Algebraic and Boolean product. **(10 Marks)**

b. Explain Reed-Muller expansion technique with the help of an example. **(10 Marks)**

Module-3

5 a. Explain with the help of examples the concept of redundancy in the synthesis of random pattern testable combinational circuits. **(10 Marks)**

b. Explain the three kinds of faults that can normally occur in PLAs. Explain the easily testable PLA design proposed by Fujiwara. **(10 Marks)**

OR

6 a. Explain the testing of sequential circuits as iterative combinational circuits. **(10 Marks)**

b. The state table of a sequential machine is given in Fig.Q6(b). Find :

i) Response of the machine for the sequence 010

ii) Homing tree.

Present state	Input	
	x = 0	x = 1
A	B, 1	C, 0
B	A, 0	D, 1
C	B, 0	A, 0
D	C, 1	A, 1

Fig.Q6(b) **(07 Marks)**

c. Explain briefly the three phases of a checking experiment. **(03 Marks)**

Module-4

7 a. Explain how testability can be improved by using Ad Hoc design rules. **(10 Marks)**

b. Explain the concepts of controllability and observability in the design of testable sequential circuits. **(10 Marks)**

OR

8 a. Explain Level-Sensitive Scan Design (LSSD) with the help of suitable diagrams. **(10 Marks)**

b. Explain Random Access Scan technique with the help of suitable diagrams. **(10 Marks)**

Module-5

9 a. Explain Pseudo–Random Pattern generator for BIST with a suitable example. **(10 Marks)**

b. Explain BILBO and STUMPS with reference to built-in-self-test (BIST). **(10 Marks)**

OR

10 a. Explain RAM fault models with the help of a schematic block diagram. **(10 Marks)**

b. Explain any four test algorithms for RAMs. **(10 Marks)**

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