CBCS SCHEME

USN | | | | | | | | | | |

20EVE21

Second Semester M.Tech. Degree Examination, Feb./Mar. 2022
Design of Analog and Mixed Mode VLSI Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain channel length modulation and body effect, with the help of a suitable figure derive the expression for :
i) Output resistance 'V_0'
ii) Body effect transconductance 'g_{mb}'. **(10 Marks)**

b. Explain the three second order effects in a MOSFET. Explain how the drain current equation is modified by the three effects. **(10 Marks)**

OR

2 a. Show a circuit for a common source stage with source degeneration and derive expressions for voltage gain under the influence of body effect and channel length modulation. **(10 Marks)**

b. Find the expression for voltage gain of a common source stage that has a resistive load by using :
i) Analytical method
ii) A small signal model. **(10 Marks)**

Module-2

3 a. Explain the folded cascade structures with proper biasing, and give their large signal characteristics. **(10 Marks)**

b. Find the expression for small signal gain of a source follower by using :
i) Analytical method
ii) A small signal model. **(10 Marks)**

OR

4 a. Explain the large signal characteristics of a folded cascade stage with the help of a circuit diagram. **(05 Marks)**

b. Calculate V_{out}/I_{in} and output impedance of the circuit shown in Fig.Q4(b). Assume that the input current source has an output impedance of R_P.

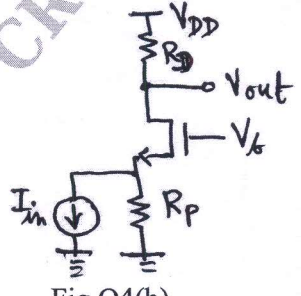

Fig.Q4(b) **(05 Marks)**

c. Derive the expression for small signal gain $A_V = g_m(1 + \eta)R_0$ for a MOSFET common gate stage. **(10 Marks)**

Module-3

5 a. Explain the operation of a basic current mirror giving the relevant equations. Explain how channel length modulation effect is eliminated in the current mirror. **(05 Marks)**

b. Explain the operation of a cascade current mirror with the help of a diagram. **(10 Marks)**

c. Explain the implementation of a two step op-amp by using MOSFETs. **(05 Marks)**

OR

6 a. Draw circuit diagrams of single stage and 2-stage op-amps and explain their operation. Compare their topology and performance. **(10 Marks)**

b. Explain the operation of an active current mirror with the help of circuit diagram. Also explain the small signal analysis of the current mirror. **(10 Marks)**

Module-4

7 a. Write short note on :
i) Noise in op-amps
ii) Jitter in PLLs. **(10 Marks)**

b. Why is Common Mode Feed Back (CMFB) required in high gain differential amplifiers? Explain the operation of CMFB with resistive sensing. What is the main drawback of CMFB with resistive sensing, and what is the solution to overcome it? **(10 Marks)**

OR

8 a. Write brief notes on :
i) Slow rate in op-amps
ii) Charge pump PPLs. **(10 Marks)**

b. Explain the non-ideal effects in PLLs. **(10 Marks)**

Module-5

9 a. Explain the operation of pipeline DAC with the help of a diagram and an example. **(10 Marks)**

b. Explain the operation of successive approximation ADC with the help of a diagram and an example. **(10 Marks)**

OR

10 a. Explain the operation of charge scaling DAC with the help of a diagram. Derive an expression for the output voltage of the DAC. **(10 Marks)**

b. Explain briefly with diagram :
i) Flash ADC
ii) Pipeline ADC. **(10 Marks)**

* * * * *