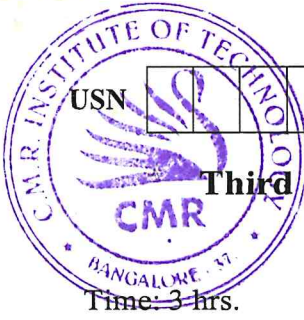


# CBCS SCHEME

15CS32



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## Third Semester B.E. Degree Examination, July/August 2022 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 80

**Note:** Answer any FIVE full questions, choosing ONE full question from each module.

### Module-1

- Explain the working of N-Channel D-MOSFE with the help of neat diagram. (08 Marks)
  - Compare JFET and MOSFET. (04 Marks)
  - What are the applications of FET? (04 Marks)

OR

- With a neat circuit diagram and relevant waveforms explain the operation of relaxation oscillator. (08 Marks)
  - Explain the performance parameters of opamp. (08 Marks)

### Module-2

- Find the minimal SOP(Sum of Product) for the following Boolean functions using K – Map  
 $f(a, b, c, d) = \Sigma m(6, 7, 9, 10, 13) + d(1, 4, 5, 11)$   
 $f(a, b, c, d) = \pi M(1, 2, 3, 4, 10) + d(0, 15)$ . (08 Marks)
  - Using Quine-McClusky method find the essential prime implicant for the following Boolean expression.  
 $f(A, B, C, D) = \Sigma m(0, 1, 2, 3, 10, 11, 12)$ . (08 Marks)

OR

- What are Hazards? Explain Static – 0 and Static – 1 Hazard. (06 Marks)
  - Discuss positive and negative logic. List the equivalences between them. (04 Marks)
  - Discuss HDL implementation models with an example. (06 Marks)

### Module-3

- Implement the following function using 8 : 1 multiplexer.  
 $f(a, b, c, d) = \Sigma m(0, 1, 5, 6, 8, 12)$  (06 Marks)
  - Realize the following function using 3 : 8 decoder  
 $F_1(a, b, c) = \Sigma m(0, 4, 6)$ ,  $F_2(a, b, c) = \Sigma m(0, 5)$ ,  $F_3(a, b, c) = \Sigma m(1, 2, 3, 7)$ . (05 Marks)
  - What is magnitude comparator? Explain one bit magnitude comparator. (05 Marks)

OR

- Design seven segment decoder using PLA. (08 Marks)
  - Explain parity generators and checkers. For a 3 bit message give the expression for even parity bit. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and/or equations written eg, 42+8 = 50, will be treated as malpractice.

**Module-4**

- 7 a. Explain the working of JK master slave flip-flop using NAND gates with logic diagram and truth table. (10 Marks)  
b. Give state transition diagram and characteristic equations for SR–FF and JK–FT. (06 Marks)

**OR**

- 8 a. With neat diagram, explain ring and Johnson counter. (08 Marks)  
b. Explain With a neat diagram how shift register can be applied for serial addition. (08 Marks)

**Module-5**

- 9 a. Design mod – 8 up synchronous counter using JK–FF. (10 Marks)  
b. Write verilog code for MOD – 8 up counter. (06 Marks)

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**OR**

- 10 a. Explain binary weighted resistor D/A convertor. Mention its drawbacks. (08 Marks)  
b. Explain successive approximation type ADC. (08 Marks)

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