CBCS SCHEME

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17CS32

Third Semester B.E. Degree Examination, July/August 2022
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. What is junction field effect transistor differentiate between JFET and MOS FET. **(10 Marks)**

b. Explain the working principle of mulitivibrotor IC – 555 with neat diagram. **(10 Marks)**

OR

2 a. Compare ideal opamp and practical opamp and explain opamp performance parameters. **(10 Marks)**

b. Explain voltage to current and current to converter with neat diagram. **(10 Marks)**

Module-2

3 a. What are universal gets? Implement the universal gates using basic gates. **(06 Marks)**

b. Implement the following function using only NAND gates $\overline{(A+B)C}D$ **(06 Marks)**

c. Final SOP and POS for the following function and design
i) SOP using only NAND gates
ii) POS using only NOR gates.
$Y = F(A, B, C, D) = \Sigma m(6, 8, 9, 10, 11, 12, 13, 14, 15)$. **(08 Marks)**

OR

4 a. Simplify the following equation using Quine-McClusky method :
$Y = F(A, B, C) = \Sigma m(2, 6, 7)$. **(06 Marks)**

b. Simplify using K – map and find SOP
$Y = F(A, B, C, D) = \Sigma m(0) + \Sigma_d(8, 9, 10, 11, 14, 15)$. **(06 Marks)**

c. Explain different types of hazards and hazard covers with example. **(08 Marks)**

Module-3

5 a. What is Multiplexer? Design a 16–to–1 Mux using two 8–to– Mux and one 2–to–7 Mux. **(06 Marks)**

b. Implement the following functions using 3 : 8 decoder and an OR gate (multi input)
$F_1(A, B, C) = \Sigma m(0, 4, 6)$, $F_2(A, B, C) = \Sigma m(0, 5)$, $F_3(A, B, C) = \Sigma m(1, 2, 3, 7)$. **(06 Marks)**

c. Write a note on parity generator and charters. **(08 Marks)**

OR

6 a. Design BCD – to – Seven segment decoder using PLA. **(08 Marks)**

b. Explain different types of flip – flops with neat diagram. **(08 Marks)**

c. Write a HDL code to perform the operations of 4 to 1 multiplexer. **(04 Marks)**

Module-4

7 a. Explain JK master – slave flip – flop with neat diagram. **(10 Marks)**

b. Write characteristic equation, finite state machine and excitation table of different types of flip – flops. **(10 Marks)**

OR

8 a. What are the different types of shift registers? Explain with neat diagram. **(10 Marks)**
b. Explain ring counter with neat circuit diagram. **(06 Marks)**
c. Compare synchronous and asynchronous counters. **(04 Marks)**

Module-5

9 a. Design Mod 8 synchronous counter using JK – FF. **(10 Marks)**
b. Explain different methods used to convert analog to digital conversion. **(10 Marks)**

OR

10 a. Write R – IR ladder network working with explanation. **(10 Marks)**
b. Write short notes on :
i) D/A converters
ii) D/A accuracy and resolution. **(10 Marks)**

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