

# CBCS SCHEME

17EE34

## Third Semester B.E. Degree Examination, July/August 2022 Analog Electronic Circuits

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

### Module-1

- 1 a. Determine the Output voltage waveform for the circuit shown below in Fig. Q1(a): (06 Marks)

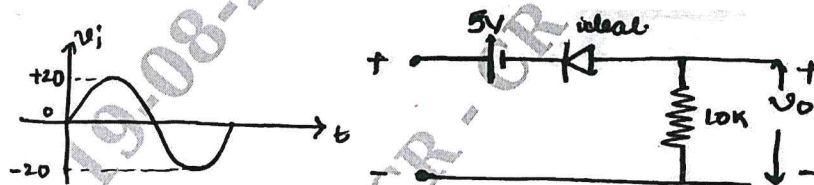


Fig. Q1(a)

- b. Sketch the Output waveform for the following input.

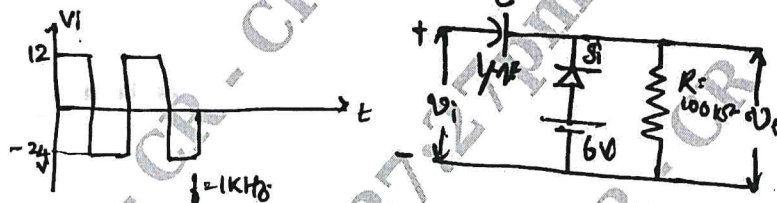


Fig. Q1(b)

- c. For the circuit shown in Fig. Q1(c), find i)  $I_C$  ii)  $V_{CC}$  iii)  $\beta$  iv)  $R_B$ . Assume  $V_{BE} = 0.7V$ . Given  $I_B = 20\mu A$  and  $I_C = 4mA$ . (07 Marks)

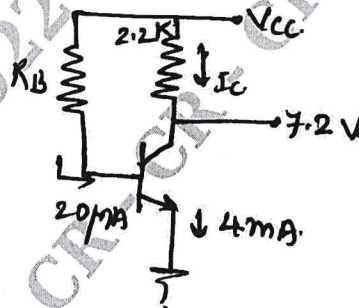


Fig. Q1(c)

OR

- 2 a. Describe the operation of a transistor as a bistable switch. (05 Marks)  
 b. Derive an expression for stability factor for a fixed bias circuit for the following : (07 Marks)  
 i)  $S(V_{BE})$  ii)  $S(\beta)$  iii)  $S(I_{CO})$   
 c. Derive an expression for a voltage divider bias circuit : (08 Marks)  
 i)  $I_B$  ii)  $V_B$ , using exact analysis.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
 2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

**Module-2**

- 3 a. Derive an expression for i) Input impedance ( $Z_i$ ) ii) Output impedance ( $Z_o$ )  
 iii) Voltage gain ( $A_V$ ) iv) Current gain ( $A_i$ ) for common emitter fixed bias configuration using hybrid  $\pi$  model. (10 Marks)
- b. A voltage source of negligible internal reactance driver a common collector transistor amplifier. The load resistance is  $2500 \Omega$ . The transistor h - parameter are  $h_{ic} = 1000 \Omega$ ,  $h_{rc} = 1$ ,  $h_{fc} = -50$ ,  $h_{oc} = 25 \mu A/v$ . Compute  $A_i$ ,  $A_v$ ,  $Z_i$  and  $Z_o$  (10 Marks)

**OR**

- 4 a. Derive an expression to verify Miller effect capacitance. (10 Marks)
- b. Derive an expression for i)  $Z_i$  ii)  $Z_o$  iii)  $A_V$  iv)  $A_i$  for a collector feedback configuration. (10 Marks)

**Module-3**

- 5 a. For the BJT cascade amplifier shown below in Fig. Q5(a) :
- Calculate the DC bias voltages and collector current for each stage.
  - Calculate the Voltage gain of each stage, the overall voltage gain and the output voltage.
  - Repeat part (ii) with a load of  $10k \Omega$  load applied to the 2<sup>nd</sup> stage.
  - Calculate the input impedance of the 1<sup>st</sup> stage and the output impedance of the 2<sup>nd</sup> stage. Take  $\beta = 200$  for both transistor. (10 Marks)

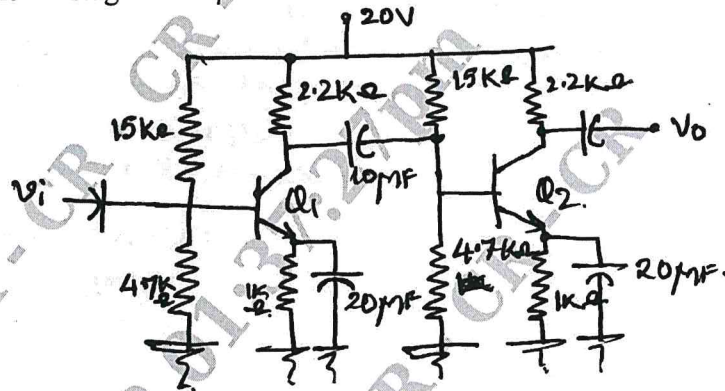


Fig. Q5(a)

- b. For the cascaded arrangement shown in Fig Q5(b), calculate :
- The loaded voltage gain of each stage
  - The total gain of the system  $A_V$  and  $A_{V1}$
  - The loaded current gain of each stage
  - The total current gain of the system.

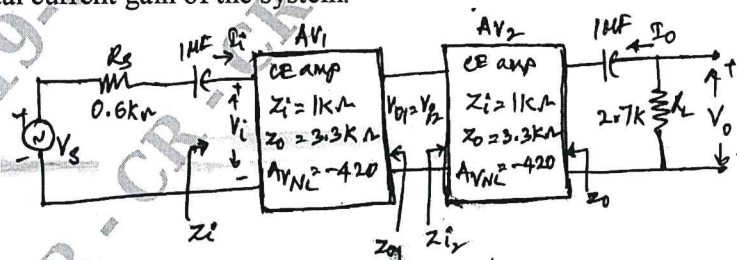


Fig Q5(b)

(10 Marks)

OR

- 6 a. With a neat diagram, explain 4 different feedback amplifier topologies. (08 Marks)  
 b. Define the general characteristics of negative feedback amplifier with appropriate mathematical formulations. (04 Marks)  
 c. An amplifier has a open loop voltage gain  $A = 1000 \pm 100$ . It is required to have an amplifier whose voltage gain varies by no more than  $\pm 0.1\%$ .  
 i) Find the reverse transmission factor  $\beta$  of feedback network used.  
 ii) Find the gain  $g$  with feedback. (08 Marks)

Module-4

- 7 a. Explain the classification of power amplifiers, with a neat waveform. (08 Marks)  
 b. Derive an expression for output power ( $P_{oac}$ ) for a transformer coupled class A power amplifier with relevant waveforms. (12 Marks)

OR

- 8 a. A crystal has the following parameters  $L = 0.334H$ ,  $C = 0.065 pF$ ;  $C_m = 1 pF$ ;  $R = 5.5k\Omega$ .  
 i) Calculate the series resonant frequency.  
 ii) Calculate the parallel resonant frequency.  
 iii) By what % does the parallel resonant frequency exceed the series resonant frequency?  
 iv) Find the Q of the crystal. (10 Marks)  
 b. Derive an expression for :  
 i) Frequency of oscillation.  
 ii) Conditions for sustained oscillations for a Wein Bridge oscillator. (10 Marks)

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Module-5

- 9 a. Explain the construction and characteristics of JFET's, with a neat diagram and characteristic waveform. (13 Marks)  
 b. Briefly explain the Transfer characteristics of a JFET, with suitable equations. (07 Marks)

OR

- 10 a. Explain the construction and characteristics of enhancement type MOSFET with relevant waveforms and appropriate diagram. (14 Marks)  
 b. Derive an expression to show the relationship between  $I_D$  and  $g_m$ . (06 Marks)

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