CBCS SCHEME

USN | | | | | | | | | | |

17EE35

Third Semester B.E. Degree Examination, July/August 2022
Digital Systems Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define combinational logic. With the help of block diagram explain combinational logic circuit. **(04 Marks)**

b. Simplify the Boolean function using K-map.

i) $f(a, b, c, d) = \Sigma m(6, 7, 9, 10, 13) + d(1, 4, 5, 11, 15)$

ii) $f(a, b, c, d) = \pi M(1, 2, 3, 4, 9, 10) + d(0, 14, 15)$. **(08 Marks)**

c. Express the following functions into canonical form :

i) $f_1 = a\bar{b} + a\bar{b} + bc$

ii) $f_2 = (a + \bar{b})(\bar{b} + c)$. **(08 Marks)**

OR

2 a. Reduce the function using K-map technique.

$f(a, b, c, d, e) = \Sigma m(1, 4, 8, 10, 11, 20, 22, 24, 25, 26) + d(10, 12, 16, 17)$. **(10 Marks)**

b. Simplify using Quine – McClusky's minimization technique

$f(a, b, c, d) = \Sigma m(1, 5, 7, 9, 13, 15) + \Sigma d(8, 10, 11, 14)$. **(10 Marks)**

Module-2

3 a. Design and implement BCD to Excess – 3 code converter. **(10 Marks)**

b. Implement full subtractor using a decoder and write a truth table. **(06 Marks)**

c. With the help of general structure, distinguish between a decoder and encoder. **(04 Marks)**

OR

4 a. Realize the following Boolean function :

$f(a, b, c, d) = \Sigma(0, 1, 3, 5, 7)$ using : i) 8 : 1 Mux ii) 4 : 1 Mux. **(08 Marks)**

b. Design a 1-bit comparator using 2 : 4 decoder giving three outputs G, E and L. **(04 Marks)**

c. Explain look ahead carry adder. **(08 Marks)**

Module-3

5 a. Explain the working of Master Slave JK flip-flop with functional table and timing diagram. Also brief about race – around condition. **(08 Marks)**

b. Obtain characteristic equation of : i) SR flipflop ii) JK flipflop iii) T – Flip-Flop. **(08 Marks)**

c. Explain the operation of SR – latch act as switch debouncer with help of the timing diagram. **(04 Marks)**

OR

6 a. Compare between Synchronous and asynchronous circuits. **(04 Marks)**

b. Explain with suitable logic and timing diagram :

i) Serial – in – Serial out shift register

ii) Parallel – in – Parallel out unidirectional shift register. **(08 Marks)**

c. Explain working of 3 – bit binary ripple counter with the suitable logic and timing diagram. **(08 Marks)**

Module-4

7 a. With the help of block diagram, explain Mealy and Moore model in a sequential circuit analysis. Give the example. **(10 Marks)**

b. Analyze the following sequential logic circuit as shown in Fig.Q7(b). Obtain the excitation and output equation, transition table and state table. Also draw the state diagram.

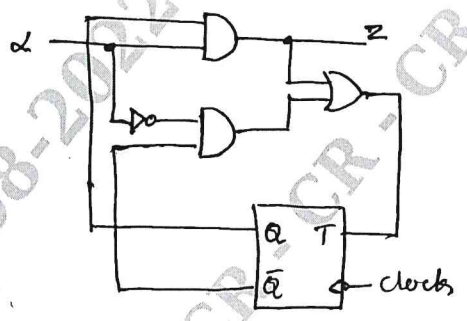

Fig.Q7(b) **(10 Marks)**

OR

8 a. Design synchronous mod-6 counter using D flip-flop to generate the sequence (0, 2, 3, 6, 5, 1, 0, - - - - -). **(10 Marks)**

b. Design a clocked sequential circuit that operates according to the state diagram shown in Fig.Q8(b). Implement the circuit using D-flip-flop.

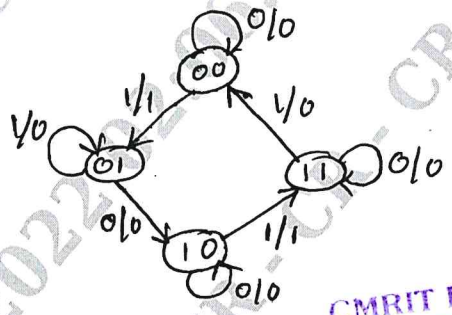

Fig.Q8(b) **(10 Marks)**

Module-5

9 a. Explain various data types of VHDL. **(08 Marks)**

b. Write the HDL code for half – adder – VHDL. **(06 Marks)**

c. Write the comparison between VHDL and verilog. **(06 Marks)**

OR

10 a. Explain brief history of HDL and structure of HDL module. **(06 Marks)**

b. Explain signal declaration in VHDL and assignment statement with example. **(06 Marks)**

c. Write the HDL code for a D – latch in VHDL and verilog. **(08 Marks)**

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