

18EE34

CMThird Semester B.E. Degree Examination, July/August 2022

Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Draw a double ended clipper circuit and explain the working principle with transfer characteristics. (08 Marks)
 - b. Explain the operation of transistor as a switch with suitable circuit and necessary waveforms. (05 Marks)
 - c. For the voltage divider bias circuit, $V_{CC}=16V$, $V_{BE}=0.7V$, $\beta=80$, $R_1=62K\Omega$, $R_2=9.1K\Omega$, $R_C=3.9K\Omega$, $R_E=680\Omega$. Calculate quiescent base, collector currents and collector to emitter voltage. (07 Marks)

OR

- 2 a. Derive an expression for SI_{CO} and SV_{BE} of emitter bias stabilization circuit. (08 Marks)
 - b. Draw and explain the working of clamper circuit which clamps negative peak of a single to zero. (06 Marks)
 - c. For the fixed bias configuration shown in Fig.Q2(c), determine I_{BQ} , I_{CQ} , V_{CEQ} and saturation level for the network. Given $V_{BE} = 0.7V$, $\beta = 50$. (06 Marks)

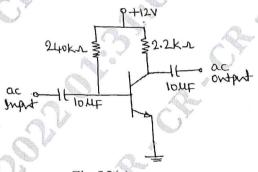


Fig.Q2(c)

Module-2

- 3 a. Compare the characteristics of CB, CE and CC configuration of transistor. (04 Marks)
 - b. Derive an expression for Z_i and Z₀ for emitter follower configuration using approximate hybrid model. (08 Marks)
 - c. A CE amplifier uses $R_L = R_S = 1K\Omega$. The h-parameters are $h_{ie} = 1.1K\Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$, $h_{0e} = 25\mu\text{A/v}$. Find voltage gain, current gain, input impedance and output admittance. (08 Marks)

OR

- 4 a. Starting from the fundamentals, define h-parameters and obtain h-parameter equivalent circuit of common emitter configuration. (08 Marks)
 - b. State and prove Miller's theorem with its dual. (08 Marks)
 - c. The h-parameters for the transistor are $h_{ie} = 1.1 \text{K}\Omega$, $h_{fe} = 99$, $h_{re} = 2.5 \times 10^{-4}$ and $h_{0e} = 25 \mu\text{A/v}$, find h-parameters for common base configuration. (04 Marks)

Module-3

- 5 a. Obtain expression for input impedance, current gain and voltage gain of a Darlington emitter follower circuit with hybrid parameter equivalent circuit. (10 Marks)
 - b. With a simple block diagram, explain the concept of feedback amplifier. (06 Marks)
 - c. The overall gain of a multistage amplifier is 100. When negative feedback is applied the gain reduces to 10. Find the fraction of the output that is feedback to the input. (04 Marks)

OR

- 6 a. With the help of circuit diagram discuss the importance of cascade connection of transistors.

 (06 Marks)
 - b. Mention the advantages of negative feedback amplifier. (04 Marks)
 - c. Using the block diagram approach, derive an expression for A_f and Z_{if} for voltage series feedback amplifier. (10 Marks)

Module-4

- 7 a. With circuit diagram, explain the operation of Wein bridge oscillator. Also derive its frequency of oscillation. (08 Marks)
 - b. With the help of circuit diagram, explain the working of Hartley oscillator. (06 Marks)
 - c. Calculate the power dissipated in the individual transistor of a class B push-pull power amplifier if $V_{CC} = 18V$ and $R_L = 4\Omega$. (06 Marks)

OR

- 8 a. Explain the operation of series fed, directly coupled class A power amplifier. Derive its efficiency interms of rms valves. (10 Marks)
 - o. State the advantage of push pull operation. (04 Marks)
 - c. A crystal has these values L=3H, $C_S=0.5pF$, $R=5K\Omega$ and $C_m=10pF$. Calculate f_s and f_p of the crystal. (06 Marks)

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- Module-5
 - a. Explain the construction, operation and characteristics of n-channel JFET. (12 Marks)
 b. Discuss the differences between FET and BJT. (04 Marks)
- c. A JFET has $g_m = 5 \text{mV}$ at $V_{GS} = 1 \text{V}$. Find I_{DSS} if pinch –off voltage $V_p = -2 \text{V}$. (04 Marks)

OR

- 10 a. With neat sketches, explain the construction operations and characteristics of n-channel depletion type MOSFET. (12 Marks)
 - b. Draw the JFET amplifier using fixed bias configuration. Derive Z_i, Z₀ and A_v using small model. (08 Marks)

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