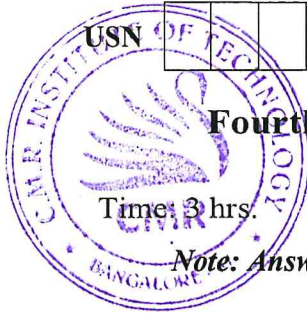


CBCS SCHEME

15EC46



Fourth Semester B.E. Degree Examination, July/August 2022

Linear Integrated Circuits

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- Discuss the effect of using resistors that are too large at the input terminals of a bipolar op-amp. Write an equation for calculating a suitable, maximum resistance value. (06 Marks)
 - Using a 741 op-amp design a non-inverting amplifier to have a voltage gain of approximately 66. The signal amplitude is to be 15 mV. (06 Marks)
 - Sketch an illustration to show the effect of op-amp slew rate and explain it. (04 Marks)

OR

- Explain the method of dealing with input offset voltage and current. (04 Marks)
 - Design an inverting summing amplifier using 741 op-amp to give the direct sum of two inputs which each range from 0.1 V to 1 V. (06 Marks)
 - Derive the expression of $V_o = \frac{R_2}{R_1}(V_2 - V_1)$ of a difference amplifier. (06 Marks)

Module-2

- Explain the operation of capacitor coupled voltage follower and also write the equations for calculating the capacitance values. (06 Marks)
 - A capacitor coupled non-inverting amplifier is to have a +24 V supply, a voltage gain of 100, an output amplitude of 5 V, a lower cutoff frequency of 75 Hz and a minimum load resistance of 5.6 K Ω . Using 741 op-amp, design a suitable circuit. (08 Marks)
 - What is the problem associated with voltage source using zener diode and how it can be solved? (02 Marks)

OR

- Design an instrumentation amplifier to have an overall voltage gain of 900. The input signal amplitude of 15 mV and supply is $\pm 15V$. Use 741 op-amp. (08 Marks)
 - Draw the fullwave precision rectifier using summing circuit and a precision halfwave rectifier and explain it with necessary mathematical analysis. (08 Marks)

Module-3

- Draw the op-amp sample and hold circuit. Sketch the signal, control and output waveforms. Explain the circuit operation. (08 Marks)
 - For the circuit shown in Fig. Q5 (b) is to handle a 1 kHz square wave input with a peak-to-peak amplitude of 6 V. Design a circuit elements using a 741 op-amp with a $\pm 12 V$ supply. Assume $V_B = 0.1 V$ and $\Delta V = 1 V$. (08 Marks)

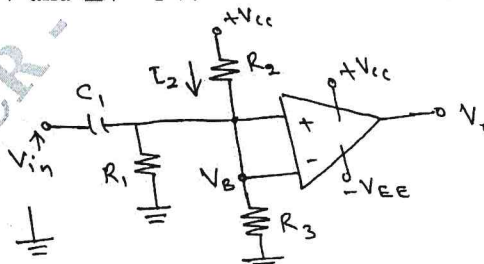


Fig. Q5 (b)

1 of 2

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

OR

- 6 a. Using a bipolar op-amp with a $\pm 18\text{ V}$ supply, design an inverting Schmitt Triggering circuit is to have $UTP = 1.5\text{ V}$ and $LTP = -3\text{ V}$. Draw input and output waveforms. Assume $R_1 = 27\text{ K}\Omega$. (08 Marks)
- b. With mathematical equations and circuits of log amplifier, explain the problem of variation of emitter saturation current and dependence of an device parameter and temperature. (08 Marks)

Module-4

- 7 a. Explain the circuit operation of second order Lowpass Filter. Write the design equations for calculating circuit elements. (08 Marks)
- b. List and explain the characteristics of a three terminal IC regulator. (08 Marks)

OR

- 8 a. Design a second order high pass active filter to have a cutoff frequency of 12 kHz . Use a 715 op-amp with $F_B(\text{max}) = 1.5\ \mu\text{A}$ and also estimate the highest signal frequency that will be passed. Assume $f_u = 11\text{ MHz}$. (04 Marks)
- b. Design an adjustable regulator from 7805 regulator to get an output voltage of 7.5 V . Assume $I_Q = 4.2\text{ mA}$ and $I_{R_1} = 25\text{ mA}$. (04 Marks)
- c. Draw the Functional diagram of 723 regulator and explain it. (08 Marks)

Module-5

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- 9 a. Draw the circuit diagram of a digital type XOR phase detector and waveforms. Explain its operation. (08 Marks)
- b. For a Astable multivibrator using 555 Timer has $R_A = 6.8\text{ K}\Omega$, $R_B = 3.3\text{ K}\Omega$ and $C = 0.1\ \mu\text{F}$. Calculate (i) t_{High} (ii) t_{Low} (iii) Free running frequency (iv) Duty cycle. (08 Marks)

OR

- 10 a. Explain the operation of a ADC using Successive Approximation. (08 Marks)
- b. Draw the block diagram of a PLL and explain it. (08 Marks)
