# CBCS SCHEME
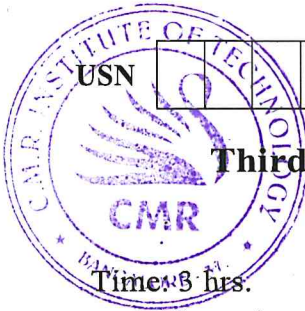
**15EC32**

## Third Semester B.E. Degree Examination, July/August 2022
## Analog Electronics

Time: 3 hrs.                                                                 Max. Marks: 80

**Note:** *Answer any FIVE full questions, choosing ONE full question from each module.*

### Module-1

**1**  a. Draw the emitter follower circuit. Derive the expressions for
   i) $Z_i$   ii) $Z_0$   iii) $A_v$.  Using $r_e$ model.                    **(08 Marks)**

   b. Draw $r_e$ and h-parameter models of a transistor in common-emitter configuration. Also give relation between $r_e$ and h-parameters.                    **(08 Marks)**

### OR

**2**  a. Derive expression for $Z_i$, $Z_0$, $A_v$ and $A_I$ for common –emitter fixed bias configuration using hybrid equivalent model.                    **(08 Marks)**
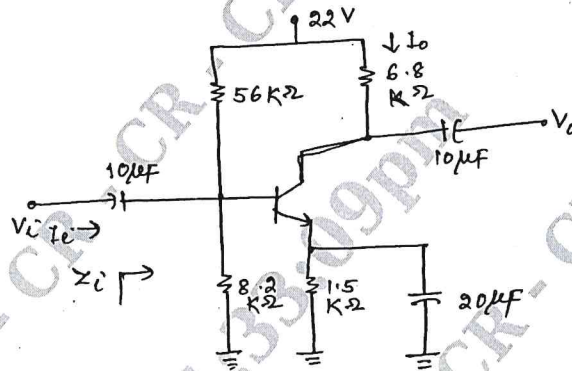
   b.



Fig Q2(b)

For the circuit shown determine : i) -$r_e$   ii) -$Z_i$   iii) $Z_0$ ($r_0 = \infty\Omega$)   iv) $A_v$ ($r_0 = \infty\Omega$).
                    **(08 Marks)**

### Module-2

**3**  a. Explain with neat diagram the construction and characteristics of a depletion type MOSFET. How a depletion type MOSFET is different than an enhancement type of MOSFET.
                    **(08 Marks)**

   b. Derive expression for $Z_i$, $Z_0$ and $A_v$ for the JFET common-source amplifier fixed bias configuration. Suing ac equivalent circuit.                    **(08 Marks)**

### OR

**4**  a. Draw JFET common drain configuration circuit. Derive $Z_i$, $Z_0$ and $A_v$ using small signal model.                    **(08 Marks)**

b. A dc analysis of the source follower network of Fig Q4(b) results in $V_{GSQ}$ = -2.86V and $I_{DQ}$ = 4.56mA. Determine : i) -gm ii) -$r_d$ iii) -$Z_i$ iv) $Z_0$ with and without $r_d$ v) $A_v$ with and without $r_d$.
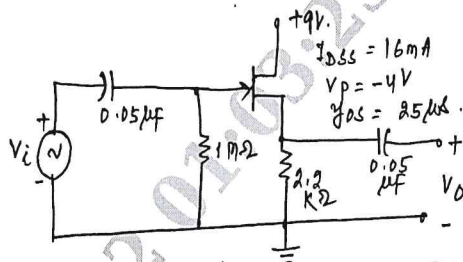


Fig Q4(b) (08 Marks)

## Module-3

5 a. Explain the low frequency response of BJT amplifier and give expression for low frequency due to I/P coupling capacitor $C_s$ and output coupling capacitor $C_c$ with neat diagram. (08 Marks)

b. Describe Miller-effect. Derive an equation for Miller input and output capacitance. (08 Marks)

## OR

6 a. Explain high frequency response of FET amplifier. Derive expression for cutoff frequencies defined by input and output circuits. (08 Marks)

b. Explain the multistage frequency effects on cutoff frequencies and the bandwidth with required waveforms and response curves. (08 Marks)

## Module-4

7 a. What are the advantages of negative feedback in amplifier? (04 Marks)

b. Derive the expression for $Z_{if}$ and $Z_{of}$ for a voltage series feedback connection with neat diagram. (06 Marks)

c. Determine the voltage gain, input and output impedance with feedback for a voltage series feedback having A = -100, $R_i$ = 10k$\Omega$ and $R_0$ = 20k$\Omega$ for feedback of $\beta$ = -0.1. (06 Marks)

## OR

8 a. What is Breackhausan's criteria for oscillation? How oscillation is generated in a circuit. (04 Marks)

b. Explain the working of a FET phase shift oscillator with neat diagram. Give the expression for oscillation. (06 Marks)

c. Draw the circuit diagram of uni-junction oscillator and explain the principle of operation and draw the characteristics curve. (06 Marks)

## Module-5

9 a. What is Power Amplifier? Explain the operation of a transformation coupled class – A power amplifier and show that maximum efficiency is 50%. (08 Marks)

b. Define voltage Regulator. Explain series and shunt voltage regulator. (08 Marks)

## OR

10 a. Explain the operation of a class – B push-pull amplifier and show that maximum conversions efficiency is 78.5%. (08 Marks)

b. For a class B amplifier using a supply of $V_{CC}$ = 30V and driving a load of 16$\Omega$, determine the maximum input power, output power, and transistor dissipation. (08 Marks)

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