CBCS SCHEME

USN | | | | | | | | | | |

15EC33

Third Semester B.E. Degree Examination, July/August 2022
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Place the following expression into proper canonical form:
i) $P = f(a, b, c) = a\bar{b} + a\bar{c} + bc$ ii) $T = f(a, b, c) = (a + \bar{b})(\bar{b} + \bar{c})$ **(06 Marks)**

b. Simplify the following using Quine-McCluskey method. Obtain the prime implicants and essential prime implicants: $P = f(a,b,c,d) = \Sigma m(4,5,6,8,9) + \Sigma d(0,7,15)$ verify using K-map. **(10 Marks)**

OR

2 a. Simplify the Boolean expression using 5-variable K-map.
$T = f(a, b, c, d, e) = \sum(0, 2, 8, 10, 16, 18, 24, 26)$. **(08 Marks)**

b. Design a 4-bit combinational circuit that generates a high output when only any of the two inputs are high. Obtain the Boolean expression. **(08 Marks)**

Module-2

3 a. Implement the full adder using 2-input NAND gates, with truth table and Boolean equations. **(08 Marks)**

b. Implement
$f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 9, 10, 15)$ using 8:1 and 4:1 multiplers. **(08 Marks)**

OR

4 a. Explain simple 4:2 encoder, with truth table. **(04 Marks)**

b. Implement $f(a, b, c) = \sum m(0, 1, 2, 5)$ using active low output dual 2:4 decoder IC74139. **(04 Marks)**

c. Explain the working principle of 4-bit parallel fast look ahead carry adder. **(08 Marks)**

Module-3

5 a. Define the following terms, and explain using a timing diagram.
i) Propogation delay ii) t_{PLH} and t_{PHL}. **(06 Marks)**

b. Explain the working of master slave J-K flipflop with logic diagram, function table, logical symbol and timing diagram. **(10 Marks)**

OR

6 a. Obtain the characteristic equations for T, D, SR and JK flipflops. **(08 Marks)**

b. With the timing diagram, explain the working of switch de bouncer, using SR latch. **(08 Marks)**

Module-4

7 a. Design a serial In serial Out unidirectional shift register and explain. **(06 Marks)**

b. Design a synchronous Mod-6 counter for the sequence (0, 2, 3, 6, 5, 1) using JK-flipflops. **(10 Marks)**

OR

8 a. Design a twisted ring counter using D flip flops, illustrate with truth table. **(06 Marks)**

b. With the help of neat block diagram, explain parallel in, serial out unidirectional shift register. **(10 Marks)**

Module-5

9 a. With a suitable example, explain Mealy and Moore model in a sequential circuit analysis. **(06 Marks)**

b. Construct the transition table, state table and state diagram in Fig.Q.9(b) for Moore Model. **(10 Marks)**

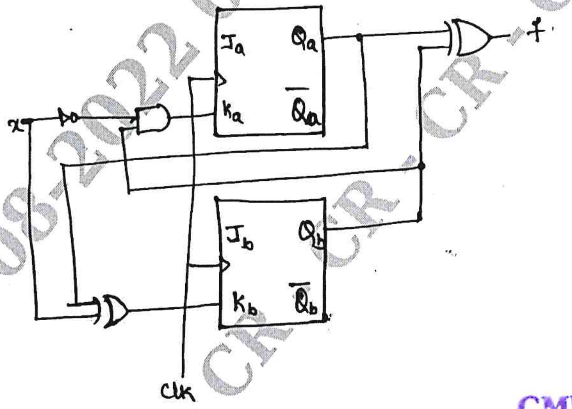

Fig.Q.9(b)

OR

10 a. A sequential circuit has one input and one output. Design a circuit using DFF for the state diagram shown in Fig.Q.10(a). **(08 Marks)**

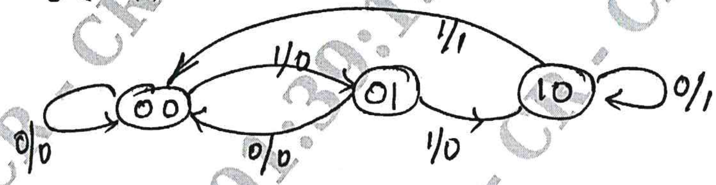

Fig.Q.10(a)

b. Construct the excitation table, transition table state table and state diagram for the sequential circuit given below in Fig.Q.10(b). **(08 Marks)**

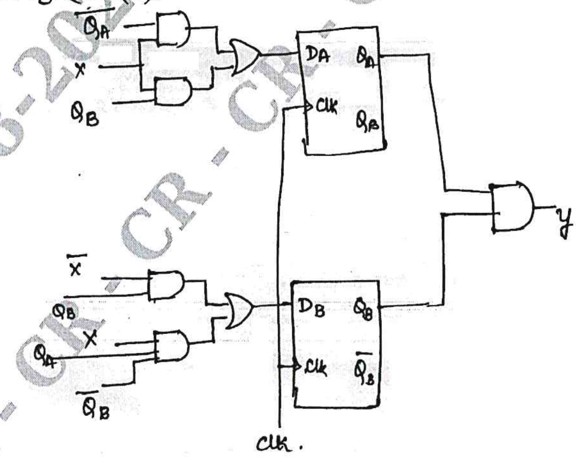

Fig.Q.10(b)

* * * * *