CBCS SCHEME

USN | | | | | | | | | | |

17EC34

Third Semester B.E. Degree Examination, July/August 2022
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Construct a truthtable and write the Boolean equations when a output variable 'z' is true when input variable a and b are true and when input variables a and c are true but b is false. **(04 Marks)**

b. Find the prime implicants and the essential prime implicants of the following Boolean function using K-Map.
i) $f(a, b, c, d) = \sum m(1, 3, 5, 7, 8, 10, 12, 13, 14) + \sum d(4, 6, 15)$
ii) $f(a, b, c, d) = \pi(0, 1, 4, 5, 8, 9, 11) + \pi d(2, 10)$ **(06 Marks)**

c. Find the minimal sum for the following Boolean function using Quine McCluskey method. $f(a, b, c, d) = \sum(2, 3, 4, 5, 13, 15,) + \sum d(8, 9, 10, 11)$. **(10 Marks)**

OR

2 a. Convert the following into proper canonical form
i) $P = (\overline{w} + x)(y + \overline{z})$ ii) $x = \overline{a}b + bc$ **(04 Marks)**

b. Find the minimal sum and minimal product for the following function using K-map $f(a, b, c, d) = \sum(6, 7, 9, 10, 13) + \sum d(1, 4, 5, 11, 15)$. **(08 Marks)**

c. Find the prime implicants of the function using Quine McCluskey method. $f(w, x, y, z) = \sum(1, 3, 4, 5, 6, 9, 11, 12, 13, 14)$ **(08 Marks)**

Module-2

3 a. Explain 4 bit look ahead carry adder with necessary diagram and relevant expression. **(10 Marks)**

b. Implement full subtractor using 74138 decoder. **(04 Marks)**

c. Implement $f(a, b, c, d) = \sum(0, 4, 8, 10, 14, 15)$ using i) 8:1 MUX with a, b, c as select line ii) 4:1 MUX with a, b as select lines. **(06 Marks)**

OR

4 a. Design 4 lines to 2 line priority encoder which gives MSB the highest priority and LSB least priority. **(06 Marks)**

b. Design a two bit magnitude comparator. **(08 Marks)**

c. Design a binary full subtractor using only NAND gates. **(06 Marks)**

Module-3

5 a. Explain the operation of switch debouncer using SR latch with the help of circuit and waveforms. **(06 Marks)**

b. What is the significance of edge triggering? Explain the working of positive edge triggered D flip-flop with their function table. **(08 Marks)**

c. Derive the characteristics equation for JK and T flip flop. **(06 Marks)**

OR

6 a. Explain the working of master slave JK flip-flop with the help of circuit diagram and waveform. **(10 Marks)**

b. Explain race around condition and how it is overcome. **(05 Marks)**

c. Explain with timing diagram (i) SR flip-flop ii) D flip-flop. **(05 Marks)**

Module-4

7 a. Design a register using positive edge triggered D flip-flop and multiplexes to operate as indicated below.

S_1	S_2	Register operation
0	0	Hold
0	1	Synchronous clear
1	0	Complement – contents
1	1	Circular shift left

(10 Marks)

b. Design a Mod 6 synchronous counter using D flip-flop to generate of sequence 0, 2, 3, 6, 5, 1, 0. **(10 Marks)**

OR

8 a. Design a 3 bit binary synchronous counter using the JK flip-flop. Write excitation table, transition table and logic diagram. **(12 Marks)**

b. With a neat diagram, explain the operation of universal shift register. **(08 Marks)**

Module-5

9 a. Explain the Mealy and Moose model of clocked synchronous sequential network. **(10 Marks)**

b. Analyse by given sequential circuit shown in Fig Q9(b), by writing input and output equations, state table and state diagram.

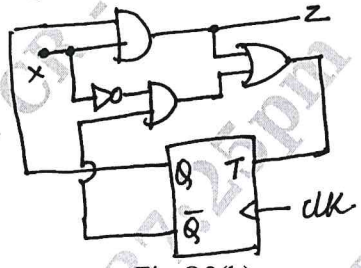

Fig Q9(b) **(10 Marks)**

OR

10 a. Design a Mealy type sequence detector to detect a serial input sequence of 101. **(10 Marks)**

b. Design a sequential circuit for a state diagram shown in Fig Q10(b) using JK flip-flop.

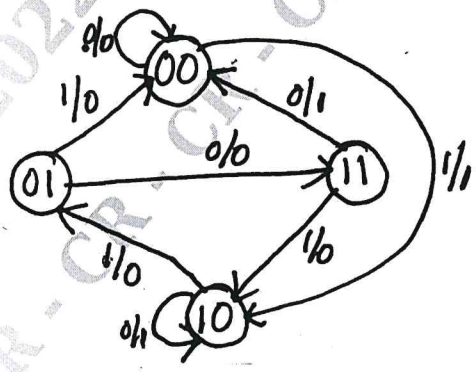

Fig Q10(b) **(10 Marks)**

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