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The design and performance of different nanoelectronic binary multipliers

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Abstract
The design and performance of digital binary multipliers built using different types of nanoelectronic devices are investigated herein. Designs for 2×2 binary multipliers implemented using different technologies such as single-electron-threshold logic (SE-TLG), hybrid single-electron transistor/complementary metal–oxide–semiconductor (SET-CMOS), and carbon nanotube field-effect transistor (CNFET) devices are elaborated and presented with corresponding simulation results. The performance metrics considered for their comparison are the power consumption, the circuit area, the propagation delay, the operating temperature, the design platform, etc. The existing CMOS-based design is also compared with all three proposed designs. The comparative analysis indicates that the SE-TLG-based 2×2 binary multiplier design exhibits very low power consumption, the smallest area requirement, and the shortest propagation delay among the three. Meanwhile, the design based on hybrid SET-CMOS devices can operate at room temperature and delivers the optimal response in terms of all the other performance metrics when compared with the other circuit implementations considered herein. Further stability analysis of the designs based on SE-TLG and hybrid SET-CMOS devices is carried out to validate their performance.

Keywords Binary multiplier · Threshold logic · Hybrid SET-CMOS · CNFET

1 Introduction

Digital multipliers are combinatorial circuits that form an integral part of any computational device. Based on the number of bits in the multiplier and multiplicand, such multipliers can be categorized as 2×2, 3×3, 4×4, etc. The length of the product depends on the length of the multiplier and multiplicand. Multipliers must be study to determine the performance of any computational device. Designing a multiplier is based on the requirement to satisfy various criteria, including low power, compact size to house more components in a limited space, reduced delay, and other parametric issues. The circuit design as well as the implementation of a multiplier thus play a very determining role in the performance of an overall computational system. The conventional approach for designing circuits using CMOS technology faces difficulties associated with the circuit area and the power consumption when scaling down below a certain limit [1], and MOS devices suffer from many disadvantages. It is possible to address the first two criteria listed above by using different nanodevices such as the carbon nanotube FET (CNFET) [2], resonant tunnel diode (RTD) [3], rapid single quantum flux (RSQF) devices [4], single-electron transistor (SET) [5–8], etc. The current work considers different potential nanoelectronic binary multiplier design based on the single-electron threshold logic gate (SE-TLG) [9–12], the hybrid SET-CMOS approach [13–15], and CNFET-based designs [16, 17]. The results are also compared with the conventional CMOS-based implementation of the same.

The basic principle of operation of single-electron devices (SEDs) is to control the movement of a single electron by controlling the gate voltage. Researchers have already proposed several circuit implementations using different SEDs

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