## Custom Precision method of Floating Point Operations of FFT Processing for Optimized Area and Delay Performance

Niharika R<sup>1</sup>

PG Student, VLSI and Embedded Systems CMR Institute of Technology Bengaluru, India nir20vlsi@cmrit.ac.in Imtiyaz Ahmed B K<sup>2</sup> Associate Professor, Dept. of ECE CMR Institute of Technology Bengaluru, India drimtiyazahmed.bk@gmail.com

Sreekantha B<sup>4</sup> Assistant Professor, Dept. of ISE HKBK College of Engineering Bengaluru, India sreekanthb615@gmail.com Niranjan L<sup>3</sup> Assistant Professor, Dept. of ECE CMR Institute of Technology Bengaluru, India niranjan11983@gmail.com

Abstract-Design of system that involves hardware implementation of signal processing algorithms poses various challenges. One such challenge is delay optimization. Typical signal processing involves various transforms for subsequent analysis in floating point representation. Fast Fourier Transform (FFT) is one of basic transform used for signal analysis. Hardware implementation of transforms or algorithms has been essential for the design of smart or autonomous systems. In this work an approach of custom precision of 12 - bit has been proposed for the FFT implementation for hardware design. From the simulation results it was observed that the proposed method has been efficient in terms of reduced delay and area for the given set of inputs. Verilog code has been considered for simulation and the obtained results were verified theoretically using Matlab. Design synthesis for delay and area has been carried out using Xilinx ISE. Proposed method has been successfully verified for better results of reduced delay of 8.191ns with reduced number of LUT's of 3149.

Index Terms-component, formatting, style, styling, insert

## I. INTRODUCTION

The technological advancements in wireless communication in terms of quality of service (QoS) is growing tremendously. Well known example of wireless communication application is all IOT based embedded devices, smart phones and so on. To provide and maintain satisfactory QoS the computational processing is expected to be fastest along with low voltage requirements. Most of the wireless based smart systems will be functioning in Real-time manner. One more attribute of the smart systems is that they are sensors based [1]. These sensors will capture the information or signals continuously and passes on to the processor which are to be processed in real time within specific deadlines. Signals or data acquired by these sensors usually of complex representation in nature. For any signal processing applications Fast Fourier Transform (FFT) would be considered as primary transformation for further analysis. FFT has been pronounced in signal processing

applications such as spectral analysis through Discrete Fourier Transform (DFT). The hardware implementation of FFT or DFT imposes design challenges of speed and memory requirements. It is due to the fact that the perceived data of floating point representation in complex number format. Implementations of complex number processing involve multiply and accumulate operation, which needs modified hardware or additional hardware. In either case the design cost would be higher and the typical approach of hardware-software separate design will affect on the time to market. With the increasing processing complexities of signal processing Field Programmed Gate Arrays (FPGAs) are preferred by the designer over conventional Digital Signal Processors (DSPs) [2]. FPGAs performance is proven to better than the DSPs in terms of execution time, along with programmable hardware supported with hardware-software co-design approach. Significance and concept of FFT or DFT has been presented in vast literature works along with different approaches for efficient and effective realisation of FFT [3]. Some of the proposes work on FFT are Pipeline FFT architectures, FFT implementation using CORDIC, High performance FFT IP cores and so on. FFT implementation has also been done by modified structure of adders and multipliers for floating point operations to achieve faster processing. One of the available methods of efficient floating point operations is customized precision of real numbers in contrary with fixed point precision as in IEEE standard of single precision (32-bit) and double precision (64bit) [4]. The approach of customized precision would be a better design option for sensor based smart system in which the size of information or signal data is pre-fixed based on the resolution or accuracy needed. For instance use of analog to digital and digital to analog converters will have fixed size or bits of resolution and precision. In such applications use customized precision would be better than fixed precision