CMR INSTITUTE OF TECHNOLOGY

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Internal Assessment Test - III

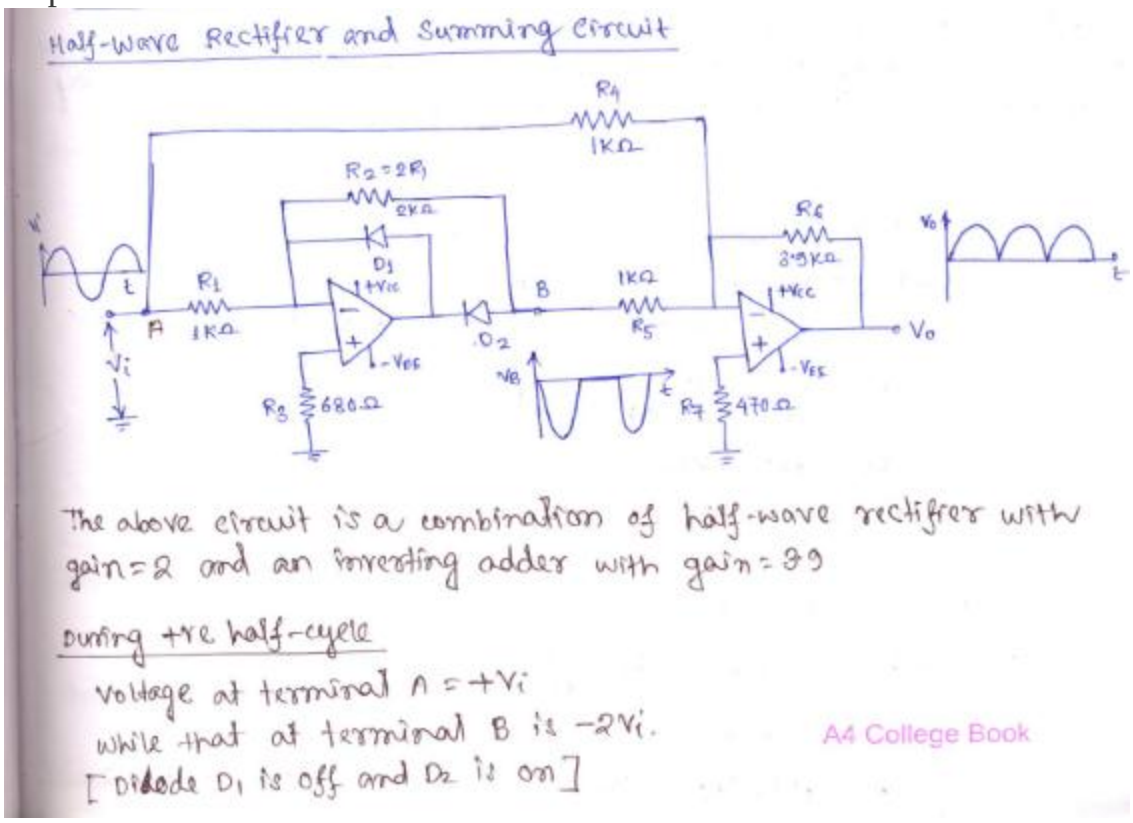
| Sub: | Operational Amplifiers and Linear IC's | | | | | | | Code: | 18EE46 |
|---|---|---|---|---|---|---|---|---|---|
| Date: | 27/08/2022 | Duration: | 90 mins | Max Marks: | 50 | Sem: | 4th | Branch: | EEE |

Answer Any FIVE FULL Questions

| | | Marks | OBE | |
|---|---|---|---|---|
| | | | CO | RBT |
| 1 | What are the major limitations of conventional rectifier? Explain the operation of precision full wave rectifier as a combination of half wave rectifier and a summing circuit. | 10 | CO3 | L2 |
| 2 | Explain the principle of operation of R-2R ladder digital to analog converter with the neat diagram. | 10 | CO4 | L2 |
| 3 | Explain the working of ADC using successive approximation method. | 10 | CO4 | L2 |
| 4 | An astable multivibrator is to be designed for getting rectangular waveform for $T_{ON}$=0.6ms,Total time period =1ms.Assume C=0.1μ F Draw the circuit diagram. | 10 | CO4 | L3 |
| 5 | Explain the working of linear Ramp ADC with necessary input and output waveform. | 10 | CO4 | L2 |
| 6 | Explain working of monostable multivibrator using 555 timer and draw its input and output waveforms. | 10 | CO5 | L2 |
| 7 | Sketch the block diagram for a basic PLL system together with the system waveforms. | 10 | CO5 | L2 |

**Solution**

1. The major limitations of these Precision Rectifiers circuits is that they cannot rectify voltages below $V_{D(ON)}$ = 0.7 V, the cut-in voltage of the diode. In these circuits $V_i$ has to rise to a threshold of the order of $V_{D(ON)}$ before any appreciable change can be seen at the output.



~~During~~ The output of the summing circuit, with $R_4 = R_5$

$$V_o = -\frac{R_6}{R_4}(V_A + V_B)$$

$$= -\frac{R_6}{R_4}(V_i - 2V_i)$$

$$= -\frac{R_6}{R_4}(-V_i) = \frac{R_6}{R_4} V_i$$

During -ve half-cycle

$V_A = -V_i$

$V_B = 0$ as $D_1$ is on and $D_2$ is off.

consequently the output is,

$$V_o = -\frac{R_6}{R_4}(V_A + V_B) = -\frac{R_6}{R_4}(-V_i + 0)$$

$$\boxed{V_o = +\frac{R_6}{R_4} V_i}$$

So, it can be seen that the output voltage is positive for both the cycle of the input voltage. If $R_6 = R_4 = R_5$ then the gain of the circuit is 1. when $R_6$ is greater than $R_4$ then rectification and amplification both occurs.

**2.**

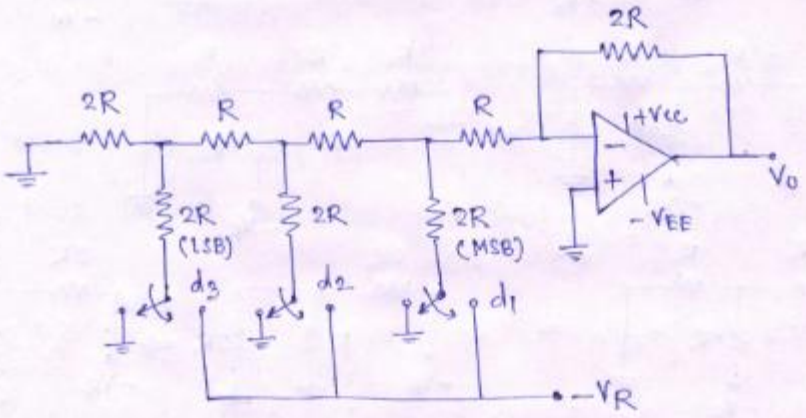



Fig- R-2R Ladder type DAC

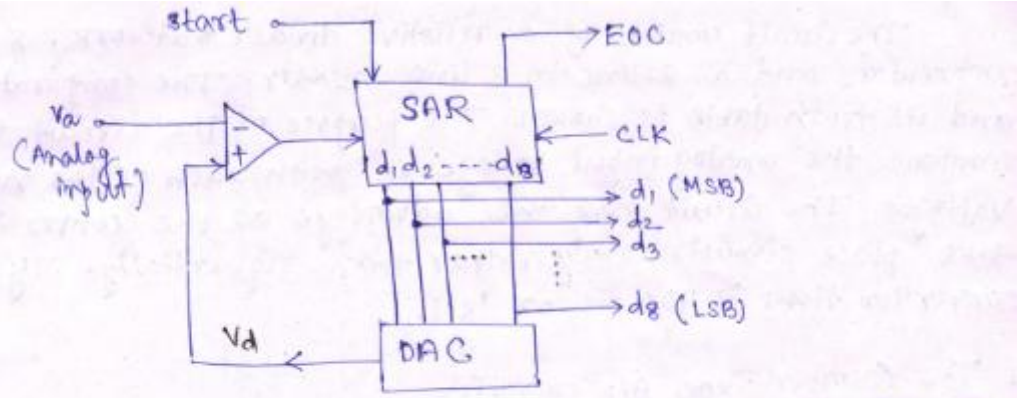
The range for R is 2·5 KΩ to 10 KΩ.

For simplicity, consider a 3-bit DAC. where $d_1 d_2 d_3$ corresponds to the binary word input to the DAC.

$-V_R$ is the reference voltage.

The feedback resistance is 2R. The network consist of R-2R network connected with the op-amp.

3.\




Functional diagram of the successive approximation ADC

| correct digital representation | Successive approximation resistor output $V_d$ at different stages in conversion | comparator output |
|---|---|---|
| 11010100 | 10000000 | 1 |
| | 11000000 | 1 |
| | 11100000 | 0 |
| | 11010000 | 1 |
| | 11011000 | 0 |
| | 11010100 | 1 |
| | 11010110 | 0 |
| | 11010101 | 0 |
| | 11010100 | |

For successive approximation type ADC, for n-bit conversion just n-clock pulses are required. An eight bit converter would require eight clock pulses to obtain a digital output. The circuit uses a successive approximation resistor (SAR) to find the required value of each bit by trial & error.

4.

Solution

$$f = \frac{1.45}{(R_A + 2R_B)C} = 1 \times 10^3$$

or, $(R_A + 2R_B) \times 0.1 \times 10^{-6} = \frac{1.45}{1 \times 10^3}$ [Assume Select. $C = 0.1\ \mu F$]

or, $R_A + 2R_B = 14.5 \times 10^3 = 14.5\ K\Omega$. ——— (1)

$$D = \frac{R_A + R_B}{R_A + 2R_B} = 0.6$$

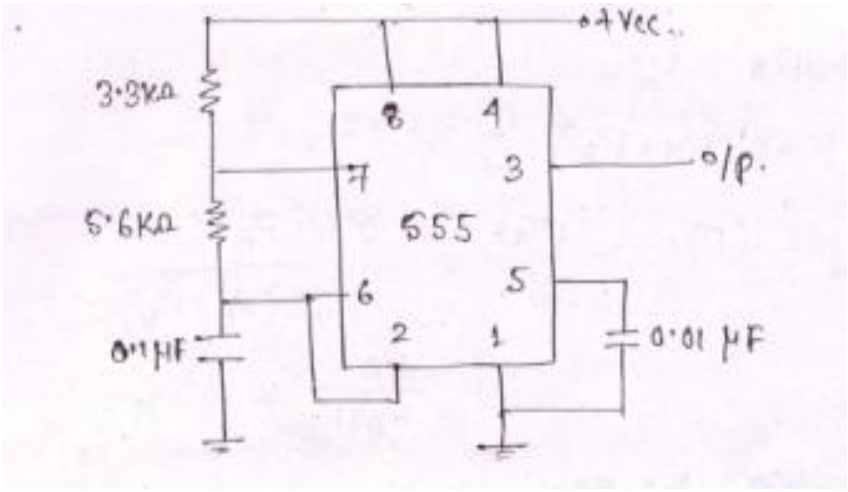
or, $R_A + R_B = 0.6(R_A + 2R_B) = 0.6 \times 14.5\ K\Omega$

$= 8.7\ K\Omega$. ——— (2)

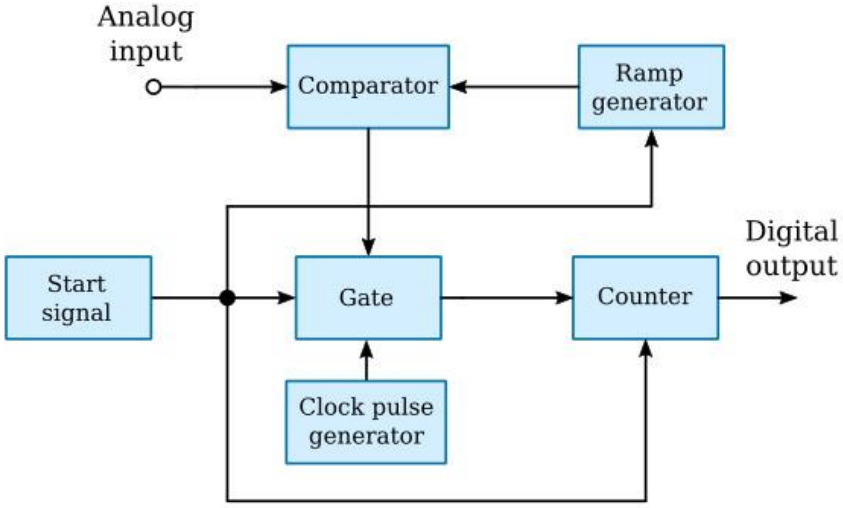
Using eq (1) and (2) we get,

$R_B = (14.5 - 8.7)\ K\Omega = 5.8\ K\Omega \simeq 5.6\ K\Omega$

$R_A = 8.7 - 5.6 = 3.1\ K\Omega \simeq 3.3\ K\Omega$.



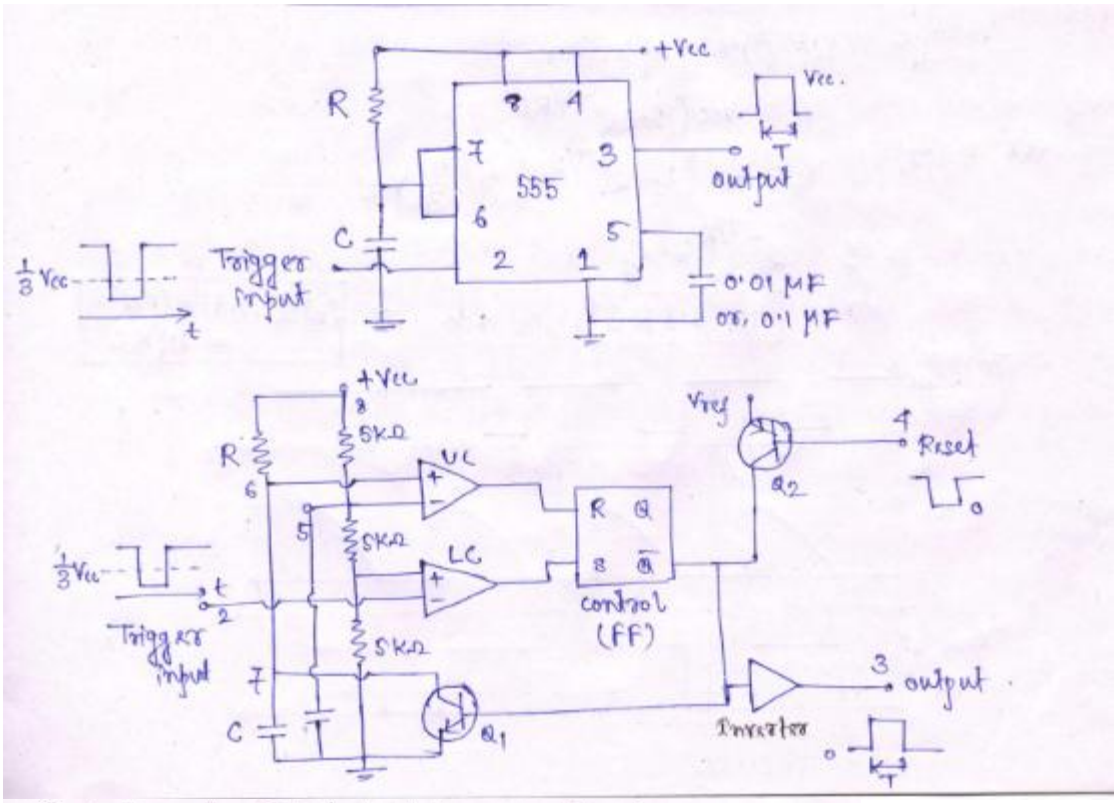

5.




Two inputs are applied to the comparator in the figure above. These are: (1) the analog input, and (2) a linear ramp (sawtooth) voltage from the ramp generator. The generator output is initiated each time a start signal is applied. The start signal also resets the counter to zero and enables the gate circuit.

As long as the analog and ramp generator inputs to the comparator differ in magnitude, the clock pulse generator will be permitted to transmit pulses at a constant repetition rate through the gate into the counter. When the two inputs to the comparator become equal (as a result of the linearly rising sawtooth) the comparator will generate a stop signal which disables the gate circuit and ends the comparison time interval. The disabled gate circuit blocks the flow of pulses from the clock pulse generator to the counter. The number of pulses accumulated in the counter during the comparison time interval is proportional to the amplitude of the analog input voltage. The counter indication is the desired digital representation of the input signal.

6.




In standby mode, FF holds transistor $Q_1$ on, thus clamping the external timing capacitor C to ground. The FF is in reset condition. $\therefore \bar{Q} = 1$, o/p = LOW.

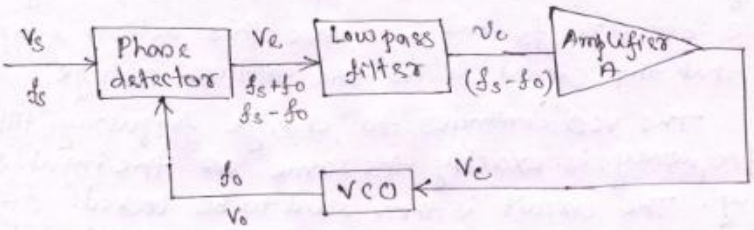
As the trigger passes through $\frac{V_{cc}}{3}$, the FF is set i.e $\bar{Q} = 0$, This makes $Q_1$ 'off' and the short circuit across the timing capacitor is released. As $\bar{Q}$ is LOW, output goes HIGH ($= V_{cc}$). The timing cycle now begins. Since C is unclamped, voltage across it raises exponentially through R towards Vcc with a time constant RC.

If the voltage across the capacitor is just greater than $\frac{2}{3}$ Vcc and the upper comparator resets the FF i.e R = 1, S = 0. This makes $\bar{Q} = 1$, transistor $Q_1$ goes on (i.e saturates), the output returns to standby state (i.e LOW).

7.

The basic block schematic of the PLL is shown. The feed system consists of

(i) Phase detector / comparator.
(ii) A low pass filter.
(iii) An error amplifier
(iv) A voltage controlled oscillator.




Block schematic of the PLL