CBCS SCHEME

USN | | | | | | | | | | |

18EE46

Fourth Semester B.E. Degree Examination, July/August 2022
Operational Amplifiers and Linear IC's

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Draw the block diagram of an Op – Amp and write the function of each block. **(08 Marks)**

b. Explain the working of Op – Amp as non – inverting amplifier. Derive the expression for its voltage gain. **(08 Marks)**

c. An Input of 3V is Fed to the non inverting terminal of an Op – Amp. The amplifier has R_i = 10 kΩ and R_f = 10kΩ. Find the output voltage. **(04 Marks)**

OR

2 a. What is an Instrumentation Amplifier? Also obtain the expression for output voltage in terms of change in Resistance ΔR using transducer bridge. **(08 Marks)**

b. Draw and explain the 2 input inverting summing amplifier and derive its output voltage equation Vo. Also explain how to convert it to an averaging amplifier. **(08 Marks)**

c. Explain the Virtual ground concept of an Op - Amp. **(04 Marks)**

Module-2

3 a. Draw the First Order Low Pass Butterworth filter and obtain its Frequency Response. **(10 Marks)**

b. Explain Working and design of voltage follower Regulator. **(06 Marks)**

c. Design a First Order Low Pass filter with a cut off frequency of 1KHz and Pass band gain of 2. Assume C = 0.001 μF. **(04 Marks)**

OR

4 a. Draw the First Order High Pass Butterworth filter and obtain its Frequency Response. **(10 Marks)**

b. With a neat circuit diagram, explain the Adjustable Voltage Regulator and its Operation. **(06 Marks)**

c. Find the Range in which output voltage can be varied with the help of 317 IC Regulator using R_1 = 820Ω and R_2 = 10KΩ potentiometer. **(04 Marks)**

Module-3

5 a. Sketch the circuit of triangular waveform generator and explain its operation. **(08 Marks)**

b. Draw and explain the Operation of Non Inverting Zero Crossing detectors. **(04 Marks)**

c. Explain the working of voltage to current converter with grounded load. **(08 Marks)**

OR

6 a. With a neat circuit diagram and waveforms, explain the Operation of inverting Schmitt trigger circuit. **(08 Marks)**

b. Give comparison between Schmitt trigger and Comparator. **(04 Marks)**

c. Explain the working of R – C phase shift oscillator using Op - Amp. **(08 Marks)**

Module-4

7 a. With a neat circuit diagram, explain the Operation of Non Saturating precision half Wave Rectifier. **(10 Marks)**

b. Explain the working of Successive Approximation Type ADC with neat sketch. **(10 Marks)**

OR

8 a. Explain the Operation of R – 2R ladder digital to Analog Converter Circuit. **(10 Marks)**

b. With a neat circuit diagram, explain the working of Precision full wave Rectifier. **(10 Marks)**

Module-5

9 a. Draw the basic block diagram of Phase Locked Loop (PLL) and explain its each component. **(10 Marks)**

b. With a neat diagram, explain the Internal Architecture of IC 555 Timer. **(10 Marks)**

OR

10 a. Draw and explain working of Monostable Multivibrator using 555 Timer and draw its Input – Output wave forms. **(12 Marks)**

b. Define the following terms related to PLL :
i) Lock range ii) Capture range iii) Pull in Time iv) Tracking range. **(08 Marks)**

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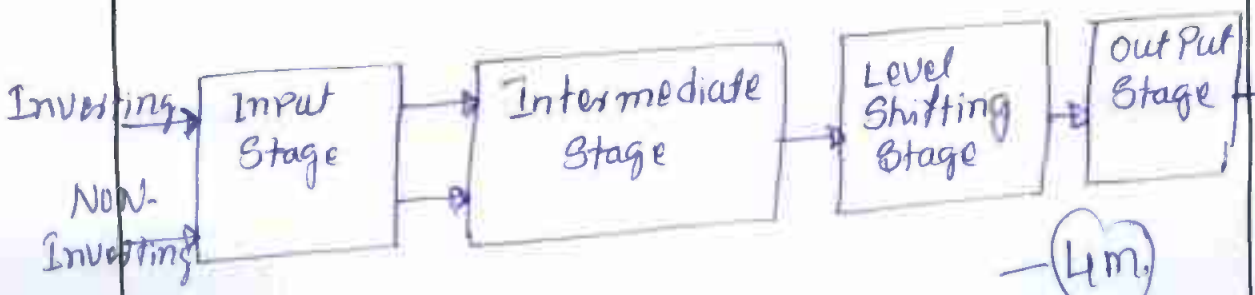
Scheme & Solutions

Signature of Scrutinizer

Subject Title : Operational Amplifier and Linear Ic's **Subject Code :** 18 EE46

Question Number	Solution	Marks Allocated
1.a	Block diagram of an OP-AMP	



(8 marks)

— 4m

Input Stage: The Input Stage is the dual input balanced output differential amplifier. This Stage Generally Provides most of the voltage gain of the amplifier and also establishes the Input resistance of OP-Amp. — 1m — 1m

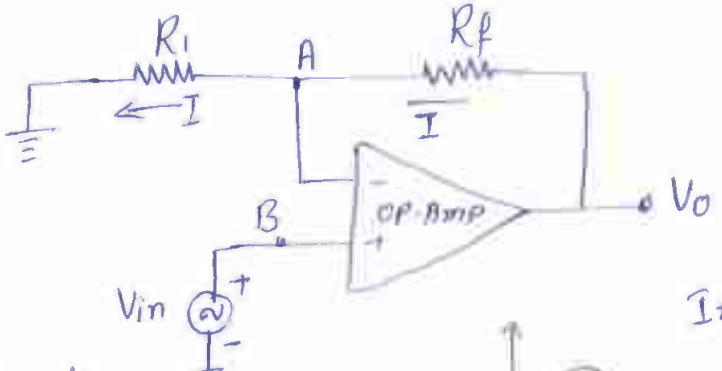
Intermediate Stage: This Stage is usually another differential Amplifier which is driven by the output of the first Stage — 1m — 1m

Level Shifting Stage: Generally the level Shifting Circuit is used after the intermediate Stage to Shift the dc level at the output of the intermediate Stage downward to Zero Volts with respect to ground. 1 m — 1m

Output Stage: This Stage Consist of Push-Pull Complementary amplifier. the Stage increase the output Voltage and rise the Current Supplying Capability of the OP-Amp. 1 M — 1m

Question Number | marks

1.b NON-Inverting Amplifier diagram



– (2 marks)

Derivation of voltage gain

The node 'B' Vin volts

hence potential at node A is same 'B' from the Concept of virtual Ground

$$V_A = V_B = V_{in}$$

$$I = \frac{V_o - V_A}{R_f}$$

$$I = \frac{V_o - V_{in}}{R_f} \quad - (1)$$

At inverting terminal I/p

$$I = \frac{V_A - 0}{R_1} = \frac{V_{in}}{R_1} \quad - (2)$$

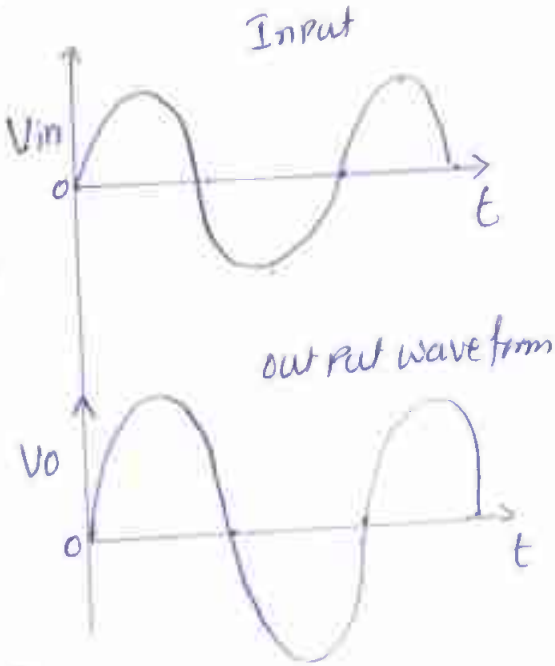
Equations (1) & (2)

$$\frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

$$\frac{V_o}{V_{in}} = \frac{R_1 + R_f}{R_1}$$

$$A_V = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}$$

– (2 marks)



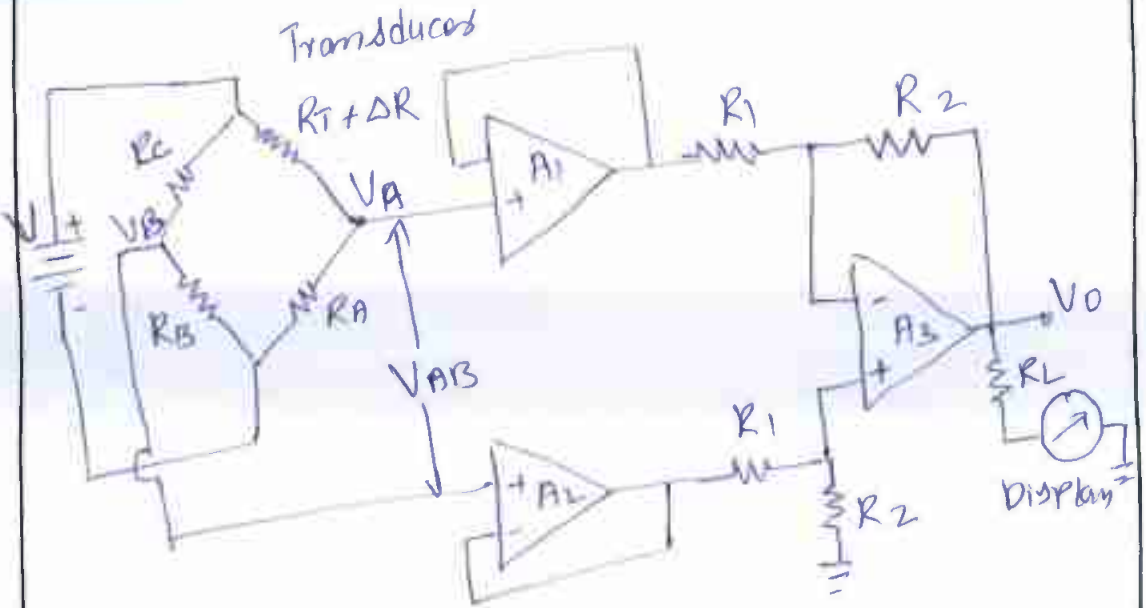
(2 marks)

— (2 marks)

2m

2m

Subject Title : Subject Code : 18EE46

Question Number	Solution	Marks Allocated
1.c	**Solution** Given data - Input voltage 3 volts Input Resistance $R_i = 10K\Omega$, feed back Resistance $R_f = 10K\Omega$ $V_o = ?$ For Non Inverting Amplifier gain $A_v = 1 + \frac{R_f}{R_1}$ —(1 Mark) $= 1 + \frac{10K}{10K}$ $= 2$ —— (1 Mark) $A_v = \frac{V_o}{V_{in}}$ $V_o = A_v V_{in}$ $= 2 \times 3$ $V_o = 6V$ —— (2 marks)	(4 marks)
2.a.	**Definition** : A special type of amplifier that is used to amplify signals of extremely low level is known as instrumentation amplifier.	(2 marks)
		2M

Marks

2.a Analysis

At Blanced condation of Bridge

$V_b = V_a$

$$\frac{VR_B}{R_B+R_C} = \frac{VR_A}{R_A+R_T} \quad -(1)$$

Let Input $V_{AB} = 0 = V_0 = 0$ — 1m

Eq(1) $\frac{R_B}{R_B+R_C} = \frac{R_A}{R_A+R_T} = \frac{R_B+R_C}{R_B} = \frac{R_A+R_T}{R_A}$

$= 1+\frac{R_C}{R_B} = 1+\frac{R_T}{R_A}$

$\therefore \frac{R_C}{R_B} = \frac{R_T}{R_A}$ - Blanced condation

Let the Physical quantity to be measured The R_T value will be change $(R_T+\Delta R)$ Then Bridge is Produce differential Input to Instrumentation Amplifier

ie $V_{AB} \neq 0$

Under this condation

$V_B = \frac{VR_B}{R_B+R_C}$ $\quad V_A = \frac{VR_A}{R_A+(R_T+\Delta R)}$ — 1m

Let $R_A = R_B = R_C = R_T = R$

$\therefore V_{BA} = V_B - V_A =$

$= \frac{VR}{2R} - \frac{VR}{2R+\Delta R}$

$V_{BA} = \frac{VR(2R+\Delta R) - VR(2R)}{2R(2R+\Delta R)}$

$V_{BA} = \frac{V.\Delta R}{2(2R+\Delta R)}$ if $V_B > V_D$ will be +ve

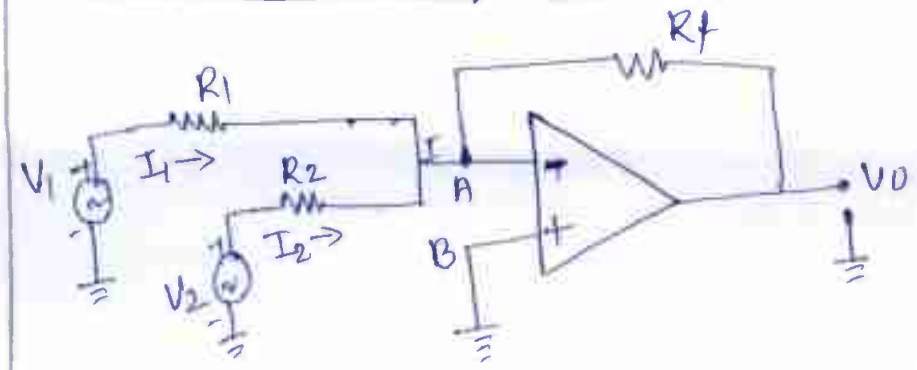
gain $A_1 = A_2 = 1$ & $A_3 = -\frac{R_2}{R_1}$

$V_0 = V_{BA} \times \frac{R_2}{R_1}$

$V_0 = \frac{V\Delta R}{2(2R+\Delta R)}\left(\frac{R_2}{R_1}\right)$ $\quad \Delta R \ll 2R$

$\boxed{V_0 \simeq \frac{V\Delta R}{4R} \times \frac{R_2}{R_1}}$ — 2m

Q.No		Marks
2.b	Inverting 2 Input Summing Amplifier CKt	



— 3m

Construction & Operation: All Input Signals to be Added are applied to the inverting input terminals of Op-Amp

— 1m

Let consider 'B' is connected to ground due to Virtual ground concept the Node 'A' is also virtual ground

Input side

$V_A = 0 \quad I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1}$ — (1)

$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2}{R_2}$ — (2)

At node A'

$I = I_1 + I_2$

output $I = \frac{V_A - V_0}{R_f} = -\frac{V_0}{R_f}$ — (3)

$V_0 = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2\right] \qquad R_1 = R_2 = R_f$

$$\boxed{V_0 = -(V_1 + V_2)}$$

— 2m

Average circuit :-

if in the inverting Summer CKt. the values of R are selected as

$R_1 = R_2 = R$

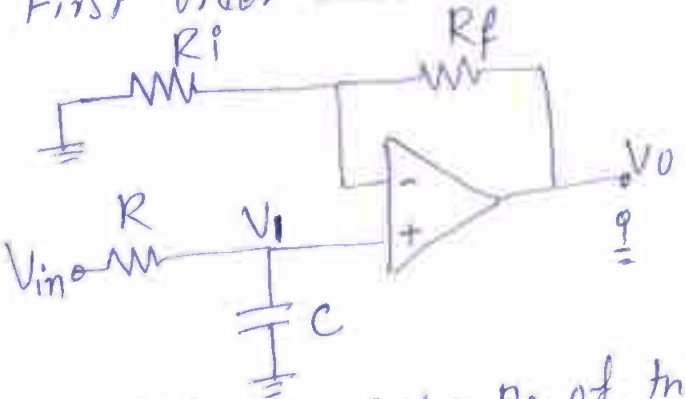
$R_f = \frac{R}{2}$

$V_0 = -\left[\frac{R/2}{R_1} V_1 + \frac{R/2}{R} V_2\right] = -\frac{V_1 + V_2}{2}$

— 2m

Subject Title :

Subject Code : 18EE46

Question Number	Solution	Marks Allocated
2 c	**Virtual Ground concept :-** The differential input voltage V_d between the noninverting and Inverting input terminals is essentially zero due to large open loop gain of OP-AMP, the difference voltage V_d at the input terminals is almost ZERO $V_0 = V_d A_{OL}$ $\quad A_{OL} \to \infty$ $\quad V_d = 0$ $V_d = \frac{V_0}{A_{OL}}$ $(V_1 - V_2) = \frac{V_0}{\infty} = 0$ $V_1 = V_2$	— 2m — 2m
3 a	First order butter worth Low Pass filter  → (2m) The closed loop gain A_0 of the OP-AMP is $A_0 = \frac{V_0}{V_{in}} = 1 + \frac{R_f}{R_i}$ — (1) $V_1 = V_{in} \times \frac{\frac{1}{sC}}{R + \frac{1}{sC}}$ $\frac{V_1(s)}{V_{in}(s)} = \frac{1}{1 + sRC}$ — (2)	— 1m — 1m

Subject Title :

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Question Number	Solution	Marks Allocated

$$H(s) = \frac{V_o(s)}{V_{in}(s)} = \left[1 + \frac{R_f}{R_i}\right] \frac{1}{1+SRC}$$

$$H(s) = \frac{A_0}{1+SRC} \quad \text{where } \omega_n = \frac{1}{RC} \qquad \text{— 1m}$$

$$= \frac{A_0}{1+\frac{s}{\omega_n}} =$$

$$H(j\omega) = \frac{A_0}{1+j\left(\frac{\omega}{\omega_n}\right)}$$

$$A(j\omega) = \frac{A_0}{1+j\left(\frac{f}{f_h}\right)} \qquad f_h = \text{UPPer cut-off frequency}$$

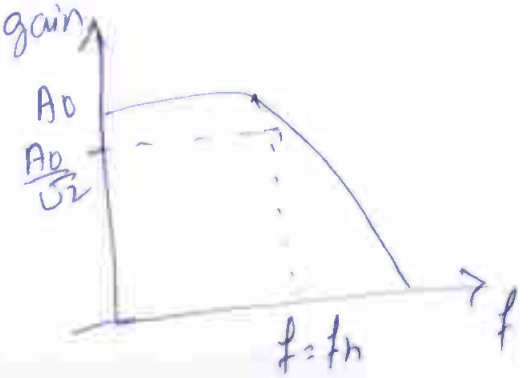
$$f_h = \frac{1}{2\pi RC}$$

$$|H(j\omega)| = \frac{A_0}{\sqrt{1+(f/f_h)^2}} \qquad \text{— 2m}$$

If $f << f_h \quad |H(j\omega)| = A_0$

$f = f_h = \frac{A_0}{\sqrt{2}}$

$f >> f_h = 0$

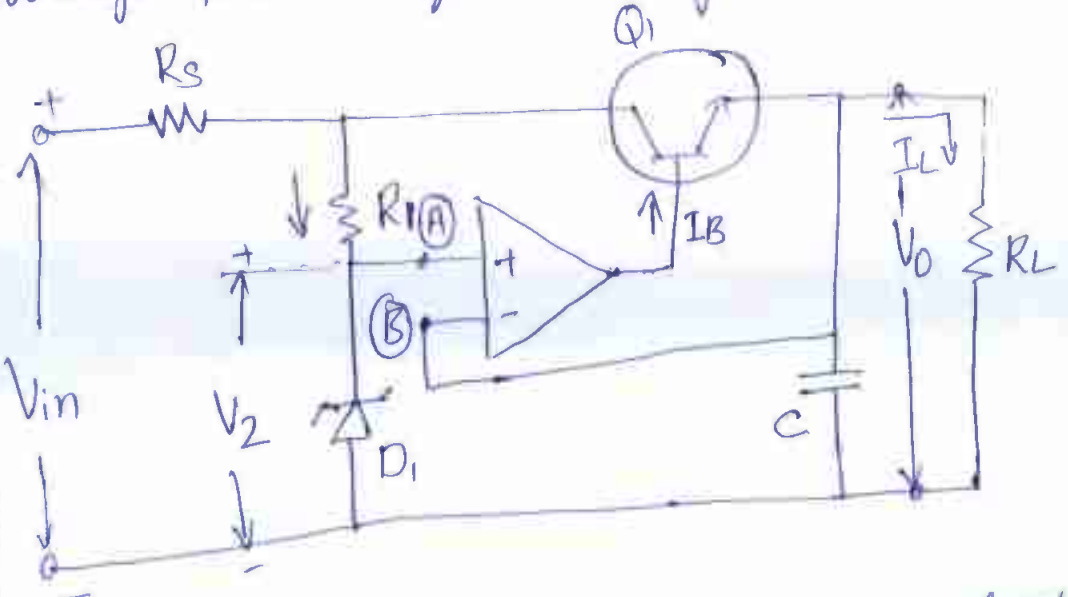


— 1m

Subject Title :

Subject Code : 186546

Question Number	Solution	Marks Allocated
3.b.	Voltage follower Regulator using OP-Amp	



.4m.

The OP-Amp is used as a comparator. The supply of OP-Amp is derived from input supply terminals. Hence OP-Amp supply voltage are +Vin and ground. the Inverting terminals of OP-Amp is connected to the output terminal

$V_B = V_O$

While the voltage at noninverting terminal node A is zener voltage V_2. — 2m

$V_A = V_2$ — 2m.

Virtual ground

$V_B = V_A$

$\boxed{V_O = V_2}$

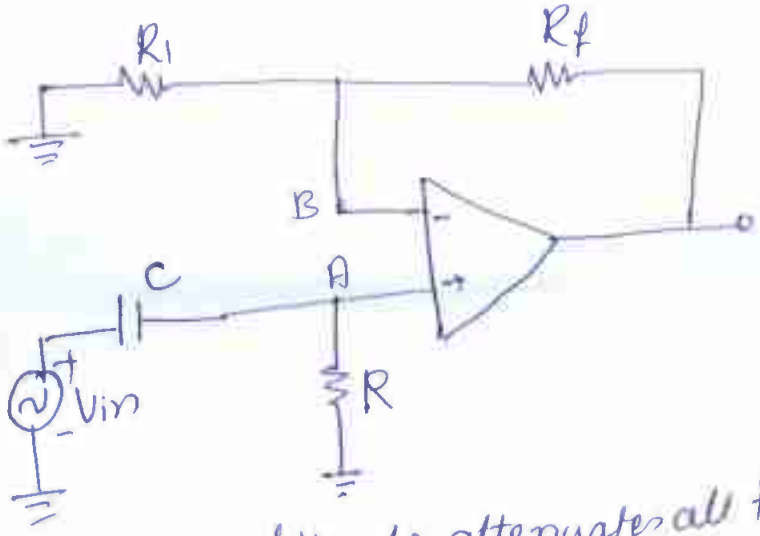
Subject Title :

Subject Code : 18EC54b

Question Number	Solution	Marks Allocated
3.c.	Low pass filter Given data f_H = 1KHz Gain $A_F = 2$ Solution : Choose C = 0.001 μF $f_H = \frac{1}{2\pi RC} = \frac{1}{2\pi \times R \times 0.001 \times 10^{-6}}$ $R = \frac{1}{2\times\pi\times 1\times10^{3}\times 0.001\times10^{-6}}$ R = 159.15 kΩ (use 150 kΩ) — (2 marks) 2M $A_F = 2 = 1 + \frac{R_f}{R_1}$ $\frac{R_f}{R_1} = 1 \quad R_f = R_1$ Choose $R_f = R_1 = 10K\Omega$ — (1 marks) 1M R_f = 10KΩ R_1 = 10KΩ 150KΩ 0.001MF Vin Vo — (1 mark) 1M	

Subject Title : Subject Code : 18EE46

Question Number	Solution	Marks Allocated
4-a	first order high Pass butterworth filter	



(4 marks)

high Pass filter is attenuates all the Signal below Specified cut-off frequency (f_L) — 1(m)

Analysis of the 1st order High Pass filter

Voltage at non inverting terminal of the OP-Amp is

$$V_A = V_{in}\left[\frac{R}{R - jX_C}\right] \qquad -jX_C = -j\left(\frac{1}{2\pi fC}\right)$$

$$V_A = V_{in}\left[\frac{-\frac{R}{jX_C}}{\left(-\frac{R}{jX_C}\right)+1}\right] = V_{in}\left[\frac{j2\pi fRC}{1+j2\pi fRC}\right] \quad (1m)$$

$$V_A = V_{in}\left[\frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right] \qquad f_L = \frac{1}{2\pi RC}$$

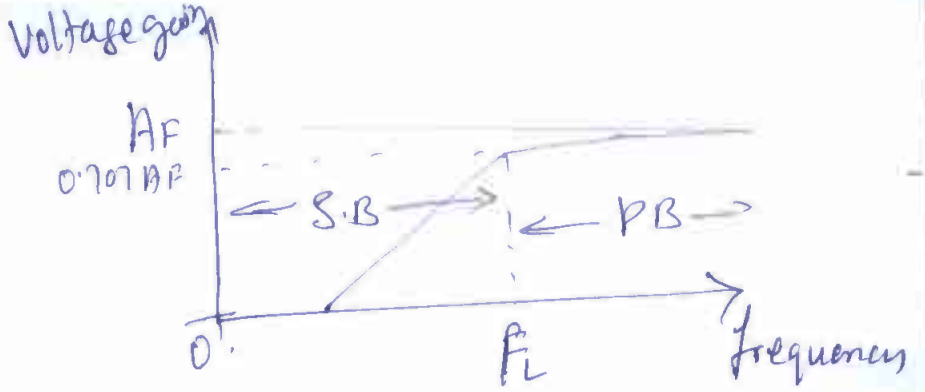
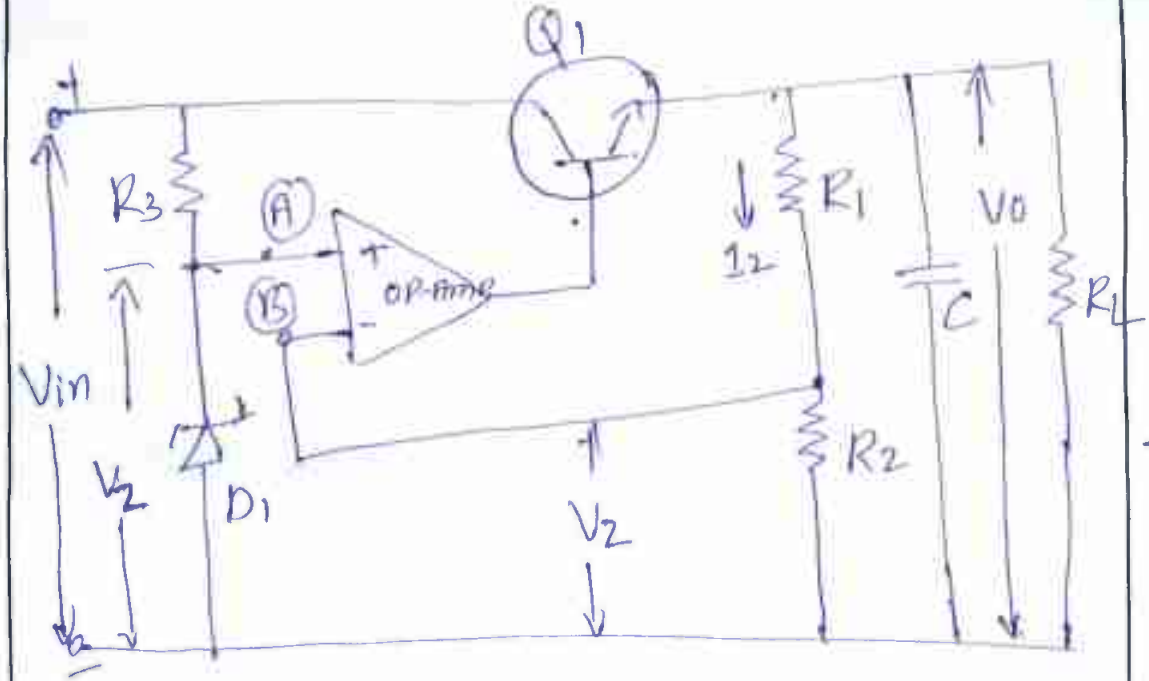
Low cutoff frequency

$V_O = A_F V_A$ $\quad A_F = \left(1+\frac{R_f}{R_1}\right)$ gain

$$\frac{V_O}{V_i} = A_F\left[\frac{1\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right] \qquad V_O = A_F V_{in}\left[\frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right]$$

Subject Title :

Subject Code : 18EC46

Question Number	Solution	Marks Allocated
	$\frac{V_o}{V_{in}} = \frac{A_F\left(\frac{f}{f_L}\right)}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}}$ — (2 marks)	2M
	① at Low frequencies $f < f_L$ $\left\|\frac{V_o}{V_{in}}\right\| < A_F$	1M
	② $f = f_L = \left\|\frac{V_o}{V_{in}}\right\| = 0.707 A_F$	
	③ $f > f_L$ $\left\|\frac{V_o}{V_{in}}\right\| \simeq A_F$	
		2M
4(b)		4M

Subject Title : Subject Code : 18ES46

Question Number	Solution	Marks Allocated

Let voltage at Non Inverting terminal is V_2

$V_A = V_2$ due Virtual ground $V_B = V_A = V_2$

V_2 is voltage across R_2. if R_2 Increase the OP-Amp output reduces Through Control Transistor.

$V_{R_2} = V_2$

$$V_{R_2} = V_2 = \frac{V_0 R_2}{R_1 + R_2}$$ — (2M)

$$V_0 = \frac{V_2(R_1+R_2)}{R_2} = V_2\left(1 + \frac{R_1}{R_2}\right)$$

to maintain constat level of voltage.

4 c. Solution:

$R_1 = 820\Omega$, $R_2 = 10K\Omega$ LM317

$I_{Adj} = 100\mu A$

When R_2 = minimum $R_2 = 0\Omega$

$$V_0 = 1.25\left[1 + \frac{R_2}{R_1}\right] + I_{Adj} R_2 = 1.25V$$ — (2 marks)

When R_2 is maximum $R_2 = 10K\Omega$

$$V_0 = 1.25\left(1 + \frac{10\times10^3}{820}\right) + 100\times10^{-6}\times10\times10^3$$

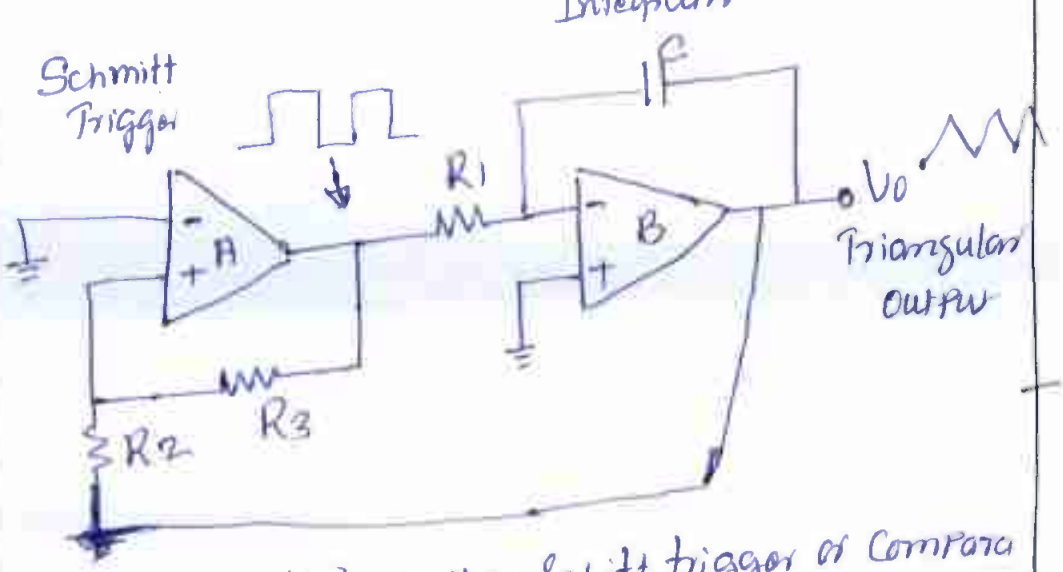
— (2 marks)

$= 17.49V$

The output voltage can be varied in the range 1.25V to 17.49V

Subject Title : Subject Code : 18EE46

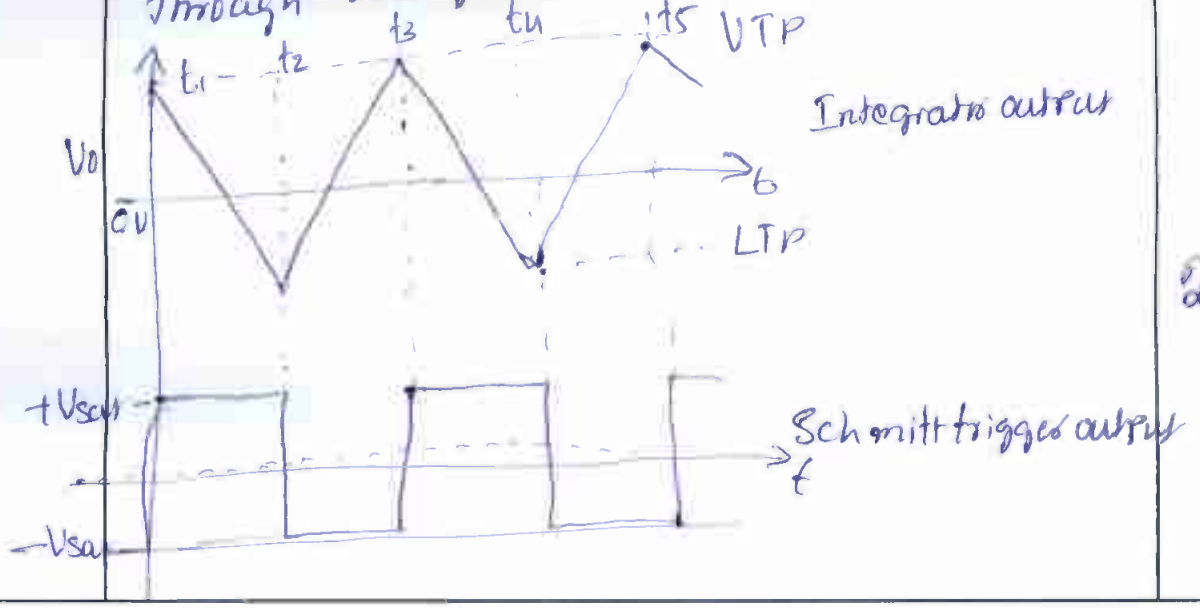
Question Number	Solution	Marks Allocated
5.a	Triangular / rectangular wave generator	



4M

The OP-Amp 'A' circuit in Schitt trigger or Compara tor while the OP-Amp B circuit is an integrator The output of Schmitt trigger is rectangular wave of amplitude ± Vsat and is applied to the inverting input of an integrator 'B' while the output of the Triangular wave generato integrator is feedback as input to Schmitt trigge through Voltage divider R2 & R3.

2M

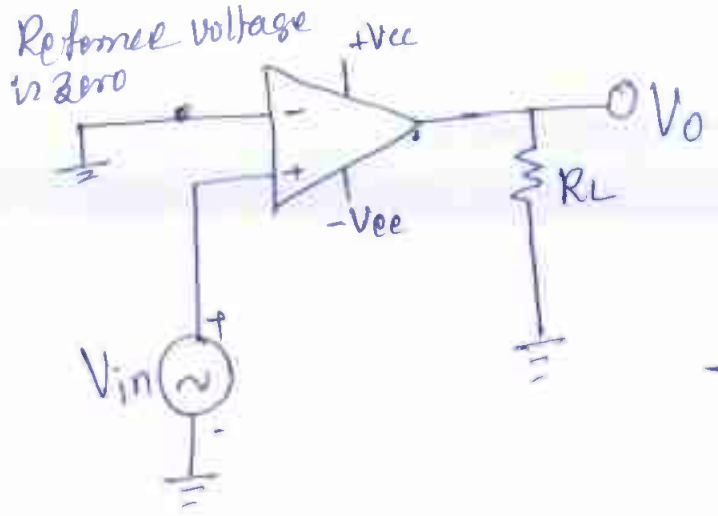


2 M

Subject Title :

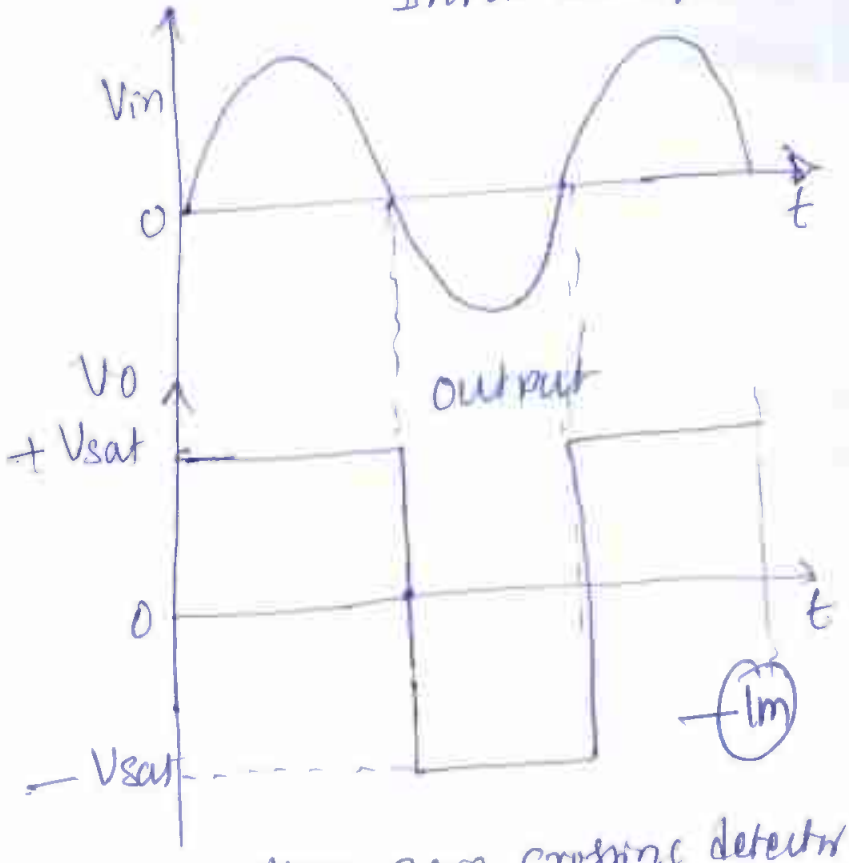
Subject Code :

Question Number	Solution	Marks Allocated
5(b)	Non Inverting Zero Crossing Detector	4m



2m

Input wave form



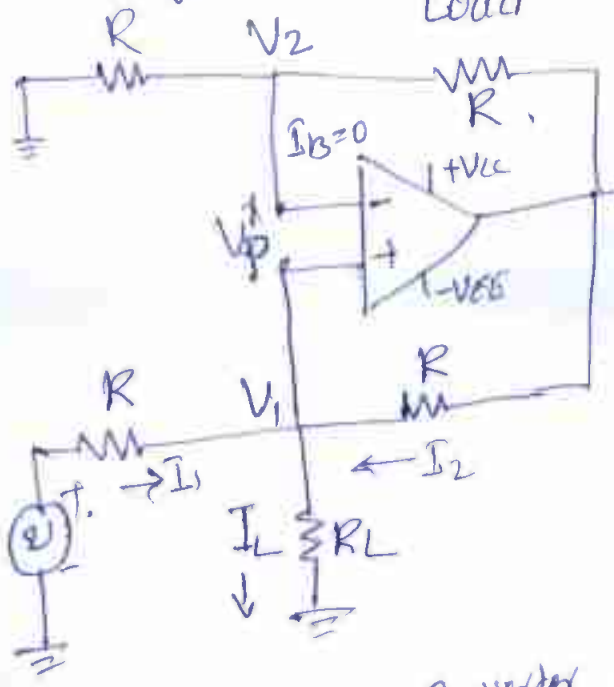
In a Non inverting zero crossing detector the OP-AMP is used in open loop mode Inverting terminal of the OP-Amp is Grounded and Input is applied to non inverting terminal. During +ve half cycle of input voltage the output voltage +Vsat During -ve cycle The output voltage -Vsat. When the Input Signal crosses the zero level. the output also Crosses zero

1m

P-14

Subject Title : Subject Code : 18EC46

Question Number	Solution	Marks Allocated
5c	Voltage to current Converter with Ground Load	8M



— (4m)

Voltage to current converter one end of the load is always grounded. the voltage at output Vin and then the relationship of the Connection between the input voltage and load current — (1m)

Apply KCL at node V_1

$$I_1 + I_2 = I_L$$

$$\frac{V_{in} - V_1}{R} + \frac{V_o - V_1}{R} = I_L$$ — (1m)

$$V_{in} + V_o - 2V_1 = I_L R$$

$$V_1 = \frac{V_{in} + V_o - I_L R}{2}$$

$$A = 1 + \frac{R_f}{R_1}$$

$$R_f = R = R_1$$

$$A = 1 + R/R = 2$$

$$V_o = 2V_1$$

$$= V_{in} + V_o - I_L R, \quad V_{in} = I_L R$$ — (2m)

$$I_L = \frac{V_{in}}{R}$$

Subject Title :

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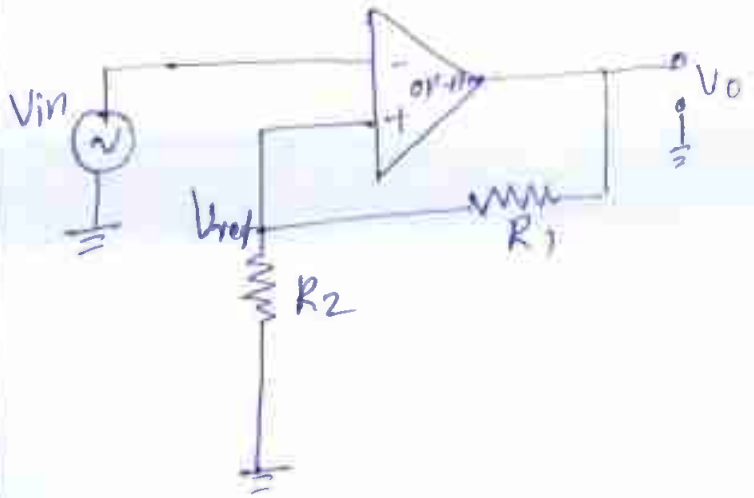
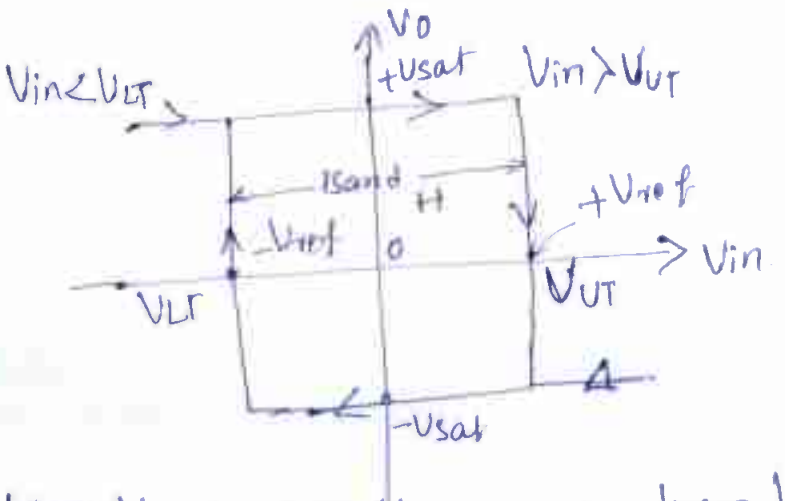
Question Number	Solution	Marks Allocated
6 a	Inverting Schmitt trigger	



— 3M.

Transfer characteristics Schmitt trigger



— 2M

When Vin is slightly positive than Vref, the output gets driven into -ve saturation -Vsat When Vin become more negative than -Vref. then output gets driven into positive saturation at +Vsat. the output voltage level change using controlled Resistance R1 & R2 — 3M

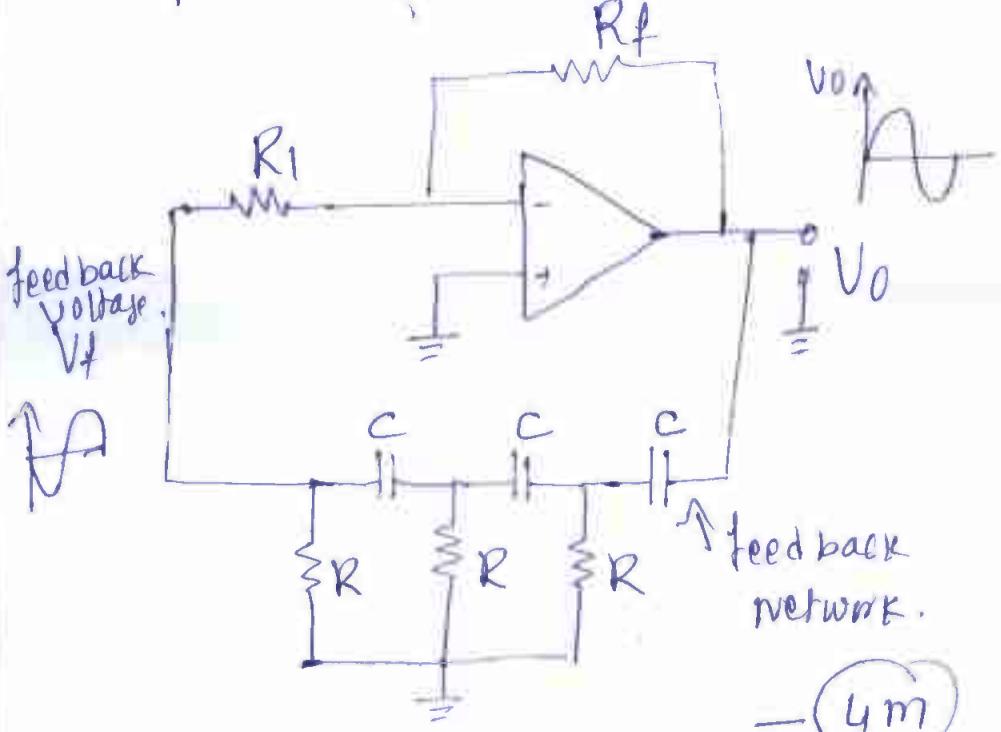
Vo = +Vsat (Upper threshold) $V_{UT} = \frac{+Vsat\ R_2}{R_1+R_2}$

Vo = -Vsat (LTP) $V_{LT} = \frac{-Vsat\ R_2}{R_1+R_2}$

Subject Title :

Subject Code : 18EE46

Question Number	Solution	Marks Allocated
6.b	Comparison of Schmitt Trigger & Comparator	
	Schmitt Trigger / **Comparator**	
	1. The feed back is used / The feed is not used	
	2. The OP-Amp used is in closed loop mode / The OP-Amp used is in open loop mode	4 marks
	3. Hysteresis exists $H = V_{UT} - V_{LT}$ / The hysteresis does not exists.	
	4. output voltage is either $+V_{sat}$ or $-V_{sat}$ / output voltage is either $+V_{sat}$ or $-V_{sat}$.	
6.c	RC Phase Shift Oscillator using OP-Amp	



— (4m)

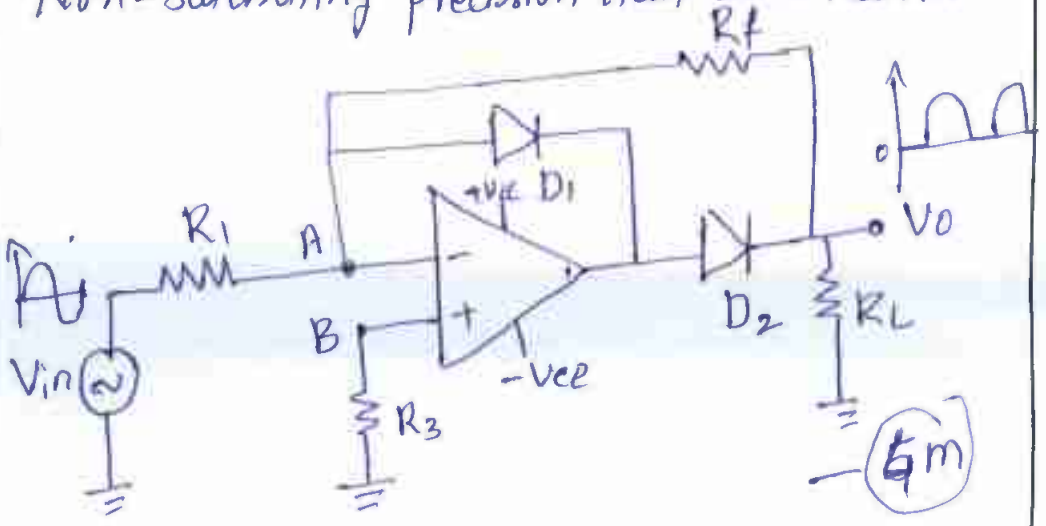
Subject Title :

Subject Code : 18EE46

Question Number	Solution	Marks Allocated
	RC Phase shift oscillator using OP-Amp in inverting mode. the phase shift of 180° between input to output. the feed back network consists of 3 RC network each section produced 60° Phase shift. Over all Phase shift Produced 360°. The frequency of oscillator circuit is given by $f = \frac{1}{2\pi RC\sqrt{6}}$ Hz — (2m) At this frequency the gain of the OP-Amp must be atleast 29 to 1 satisfy $A\beta = 1$ Gain Amplifier of OP-Amp using inverting Amplifier $\lvert A\rvert \geq \frac{R_f}{R_1} \geq 29$ $R_f \geq 29 R_1$ This is the frequency with which circuit oscillation $\beta = \frac{1}{1-5x(\sqrt{6})^2} = -\frac{1}{29}$ $\lvert\beta\rvert = \frac{1}{29}$ $\lvert A\beta\rvert \geq 1$ $\lvert A\rvert\lvert\beta\rvert \geq 1$ $A \geq \frac{1}{\lvert\beta\rvert} \geq \left(\frac{1}{29}\right)$ $\boxed{\lvert A\rvert \geq 29}$ — (2m)	8m

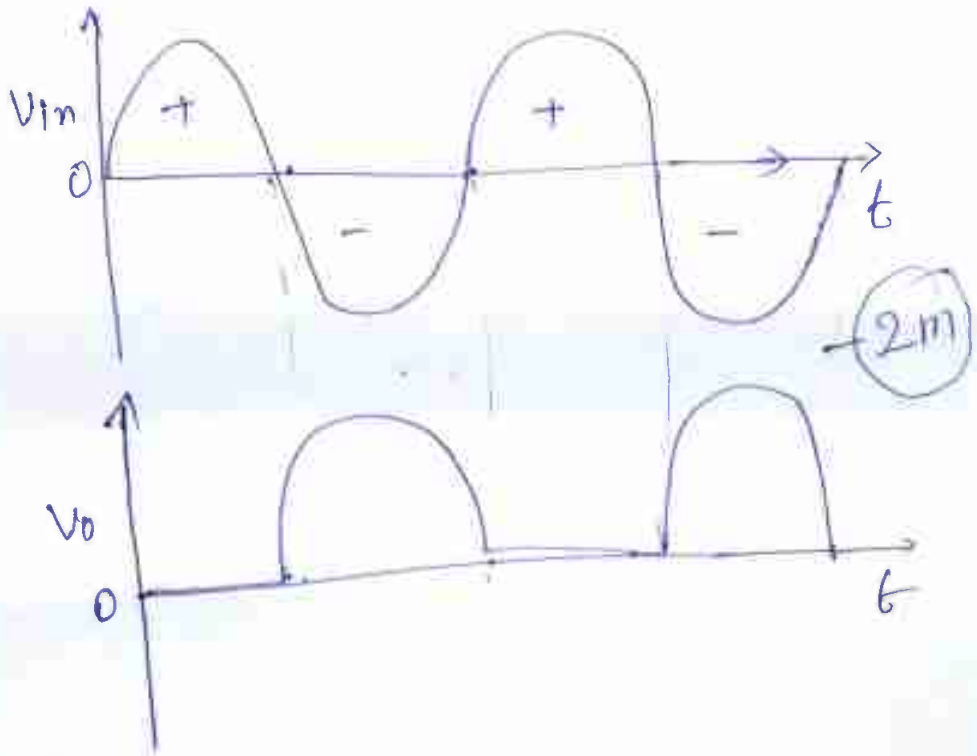
Subject Title :

Subject Code : BEE46

Question Number	Solution	Marks Allocated
7a.	Non-Saturating Precision Half Wave Rectifier  (5m)	
	Operation: When Vin is Positive the OP-Amp output goes negative thus D_2 diode is reverse biased and output is zero. the diode D_1 gets forward biased due to negative output voltage This tends to pull OP-amp inverting terminal in a negative direction. This causes OP-Amp output to go Positive. (2m)	10m
	When Vin is negative. the OP-Amp output is Positive which makes D_2 forward biased and D_1 revere biased. the circuit acts as an inverting amplifier Producing $V_o = -\left(\frac{R_f}{R_1}\right) V_{in}$ When $R_f = R_1$, then a negative half cycle of Vin Produces a Positive half cycle of Vin. (2m)	

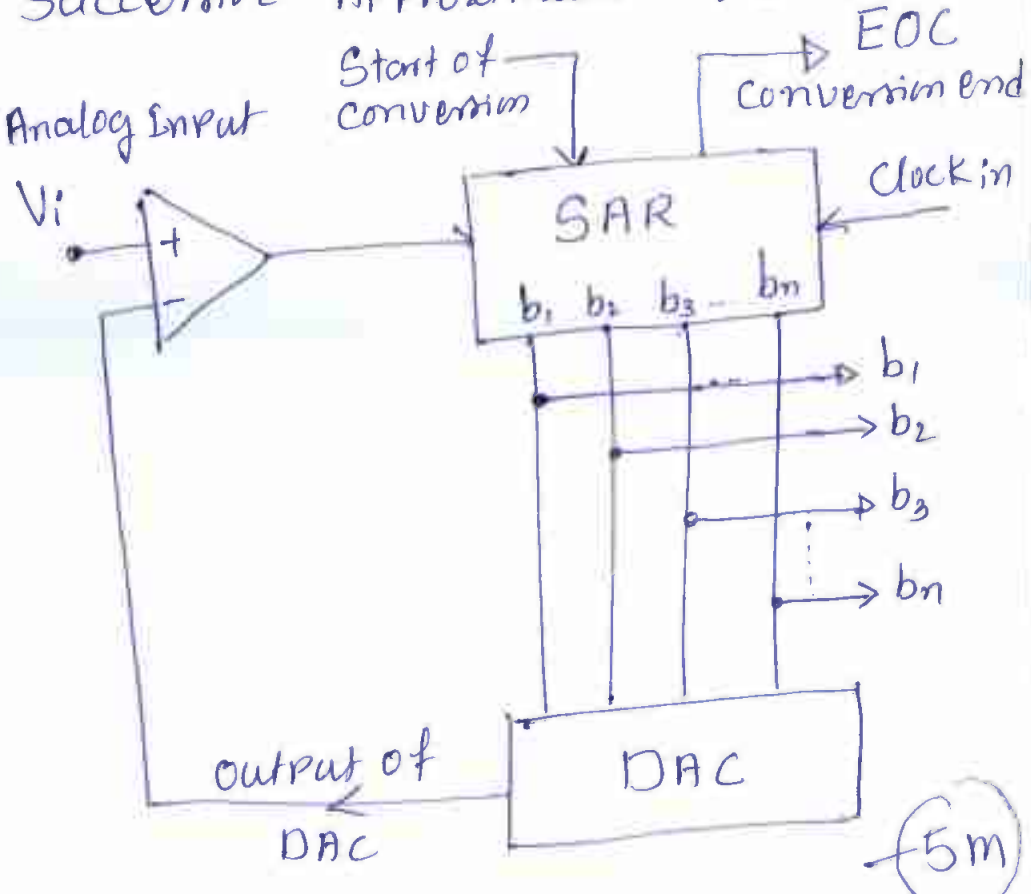
Question Number	Solution	Marks Allocated

7.a



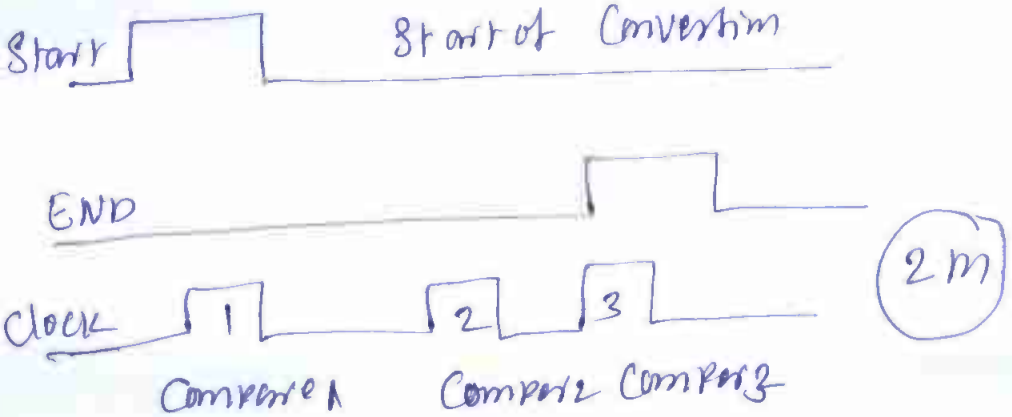
2m

7.b Successive Approximation Type ADC



5m

Subject Title : Subject Code : 18EE46

Question Number	Solution	Marks Allocated
7b	The block diagram of Successive approximation A/D Converter. It Consists of a DAC, a Comparator and a Successive approximation register (SAR) The external clock input sets the internal timing Parameters. The control Signal Start of Conversion Initiates an A/D Conversion Process and end of Conversion Signal is activated When the Conversion Completed. — (3m)  (2m)	10m

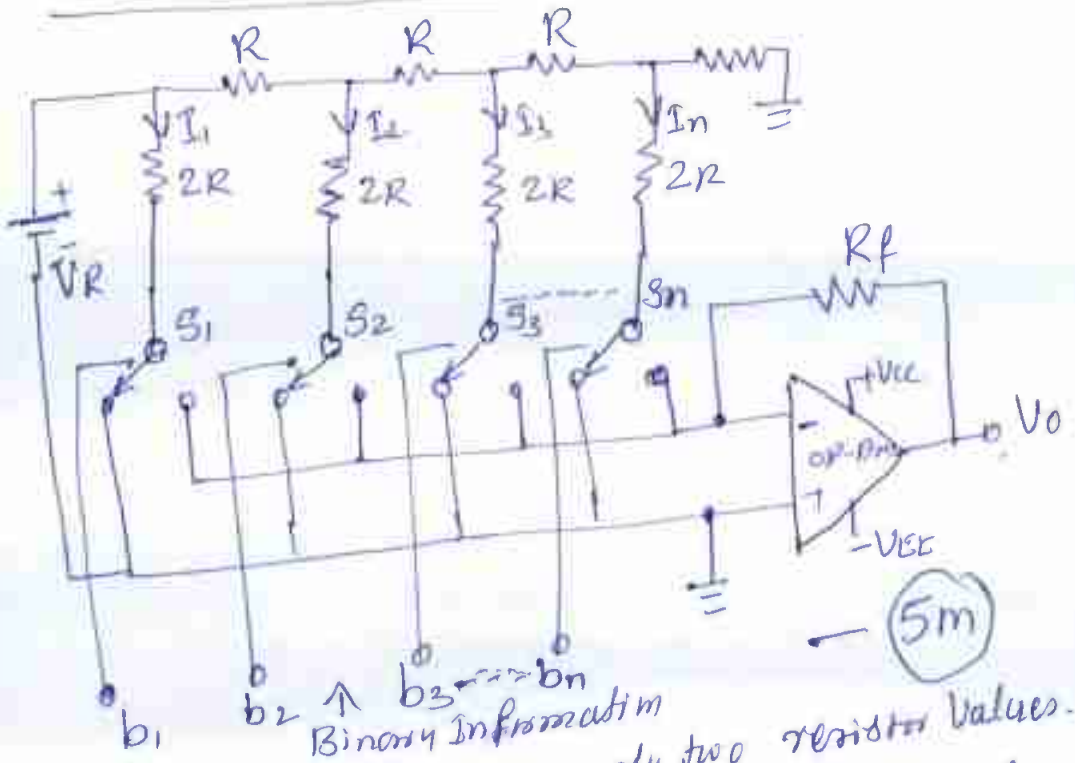
Subject Title :

Subject Code : 18EE46

Question Number	Solution	Marks Allocated

8 a

R-2R Ladder DAC



— 5m

Binary Information

R-2R Ladder DAC using only two resistor values. each bit of the binary word controls the corresponding switch either to ground or to the inverting input terminal of the OP-Amp which is at the virtual ground. the current flow through resistance is constant and its independent of switch position. then current can be given as — 2m

10m.

$$I_1 = \frac{V_R}{2R}, \quad I_2 = \frac{V_R/2}{2R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{I_1}{4}, \quad I_n = \frac{V_R/2^{n-1}}{2R} = \frac{I_1}{2^{n-1}}$$

output voltage V_0 is given

$$V_0 = -I_T R_f$$

$$V_0 = -R_f (I_1 + I_2 + I_3 \cdots I_n) \quad \text{— 3m}$$

$$= -R_f \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{2R} + b_3 \frac{V_R}{2R} - \frac{b_n V_R}{2^n R} \right)$$

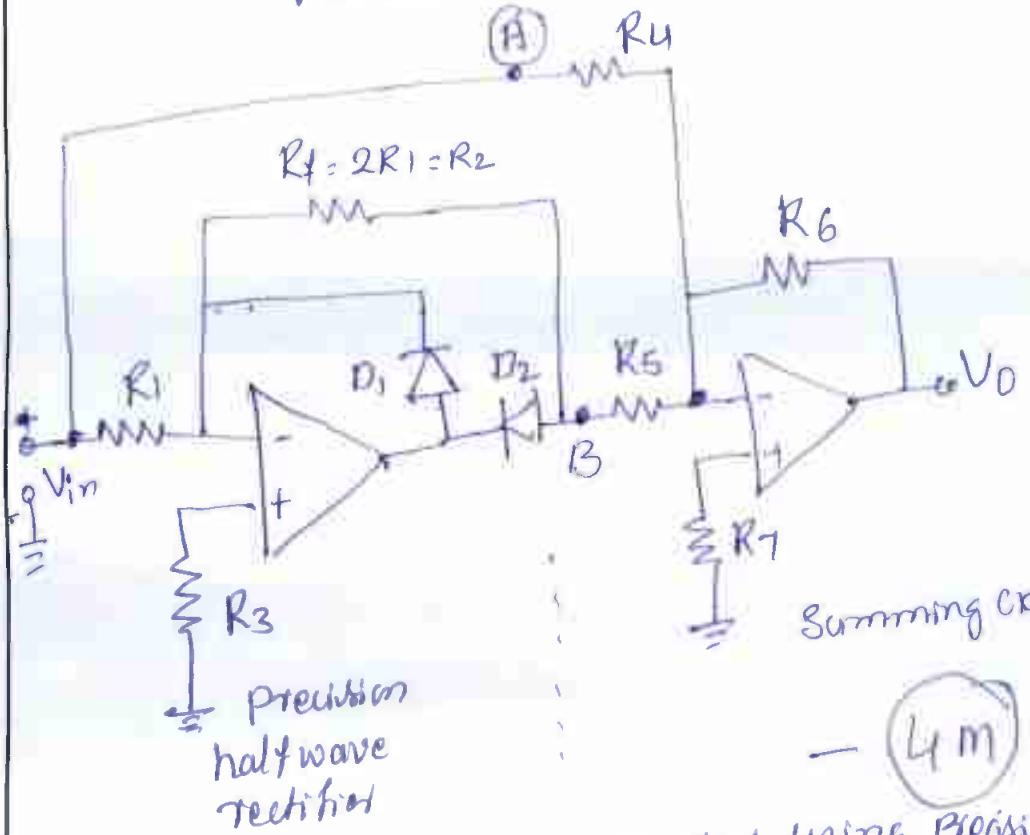
$$= \frac{-V_R R_f}{R} [b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} \ldots + b_n 2^{-n}]$$

$R_f = R$

$$V_0 = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots + b_n 2^{-n})$$

Subject Title : Subject Code : 18EE46

Question Number	Solution	Marks Allocated
8.b	Precision full wave Rectifier	10m



— (4 m)

Full wave rectifier constructed using Precision half wave rectifier & summing circuit

When V_{in} is +ve, $V_A = V_{in}$, HWR output is $V_B = -V_{in}$

$R_f = 2R_1$, V_A & V_B two inputs of Summing Amplifier

$$V_o = -\left[\frac{R_6}{R_4} V_A + \frac{R_6}{R_5} V_B\right] \cdot R_5 = R_4$$

$$V_o = -\frac{R_6}{R_4}[V_A + V_B] = -\frac{R_6}{R_4}[-V_{in}] = \frac{R_6}{R_4} V_{in}$$

for -ve cycle of V_{in}

$V_A = -V_{in}$, $V_B = 0$

$$V_o = -\left[\frac{R_6}{R_4} V_A + \frac{R_6}{R_5} V_B\right]$$

— (4m)

$$\boxed{V_o = +\frac{R_6}{R_4} V_{in}}$$

Subject Title :

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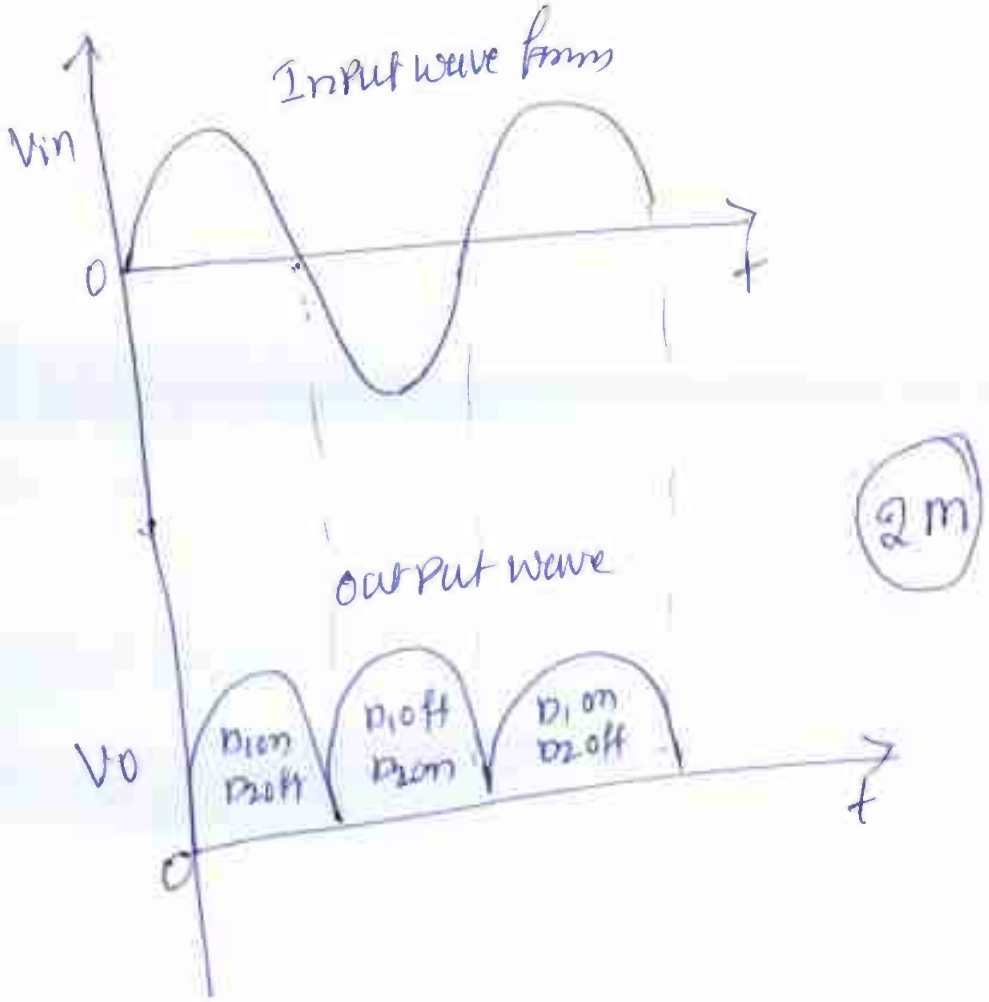
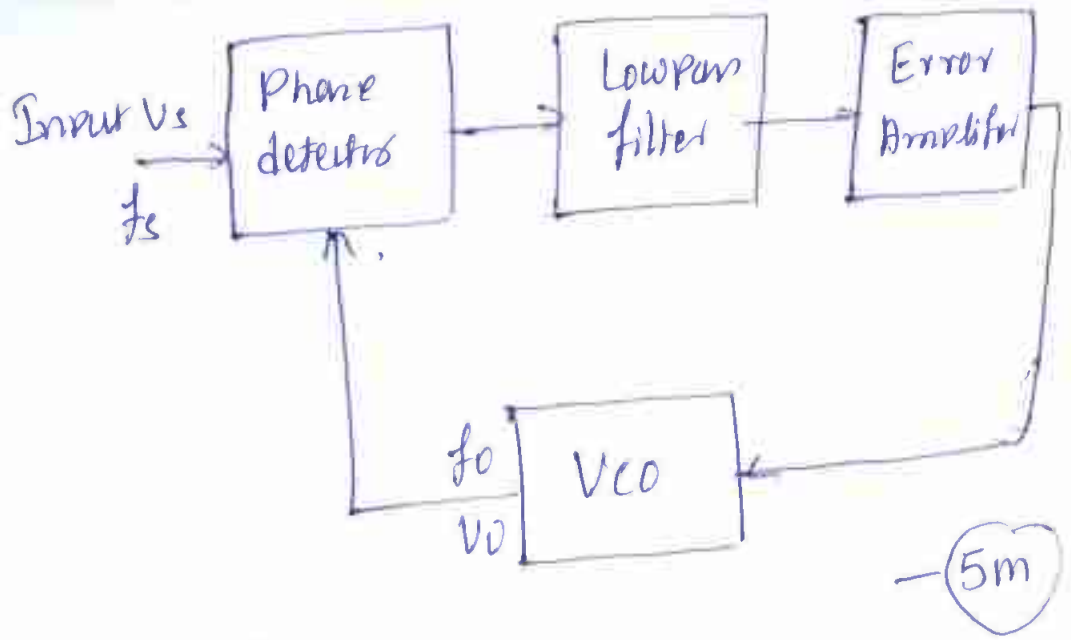
Question Number	Solution	Marks Allocated



2m

9 -a Block diagram Phase locked loop (PLL)



5m

P.T.O

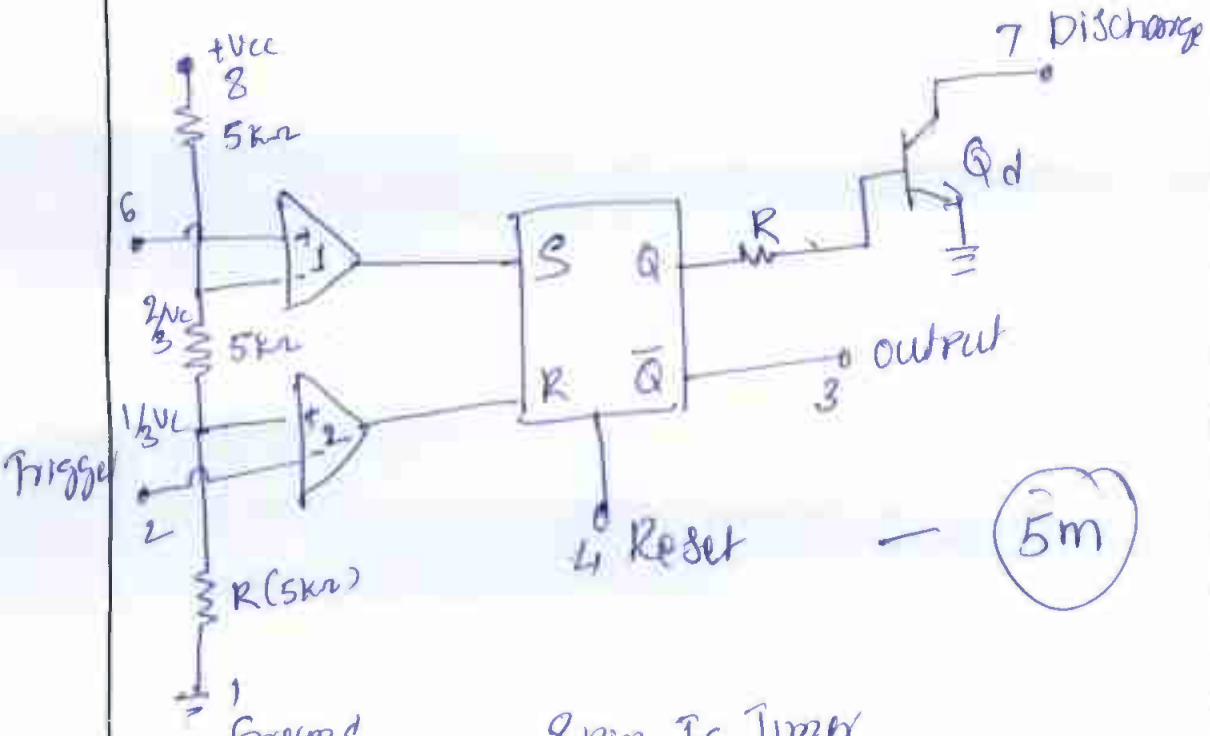
Subject Title : Subject Code : 18EE46

Question Number	Solution	Marks Allocated
9.a	PLL is basically a closed loop system designed to lock the output frequency and phase to the frequency and phase of an input signal. Operation : It consists of ① Phase detector ② Low pass filter ③ Error amplifier ④ Voltage Controlled oscillator (VCO) — (2)m The phase detector compares the input frequency f_i with the feedback frequency f_o and generates an output signal which is a function of difference between the phases of the two input signal. The output signal of the phase detector is a dc voltage. the output of phase detector is applied to low pass filter to remove high frequency noise from the dc voltage. The output of LPF without high frequency noise is often referred to as error voltage or control voltage for VCO. The VCO is an oscillator circuit in which the frequency of oscillation can be controlled by an externally applied voltage. — (3m)	10m.

Subject Title : Subject Code : 18EE46

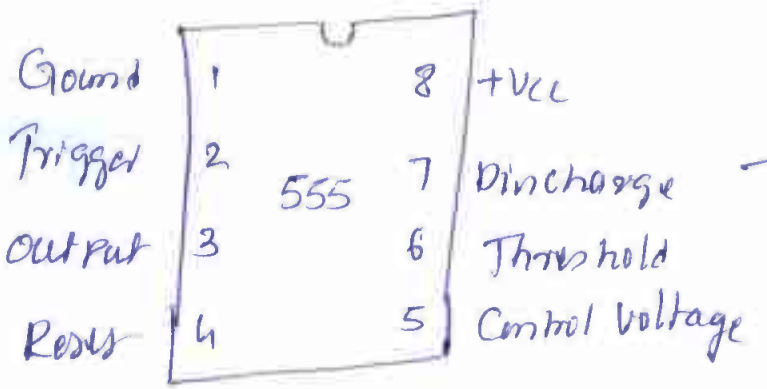
Question Number	Solution	Marks Allocated

Q. b Block diagram of Internal Structure of 555 Timer



5m

8 Pin IC Timer



1m

10m.

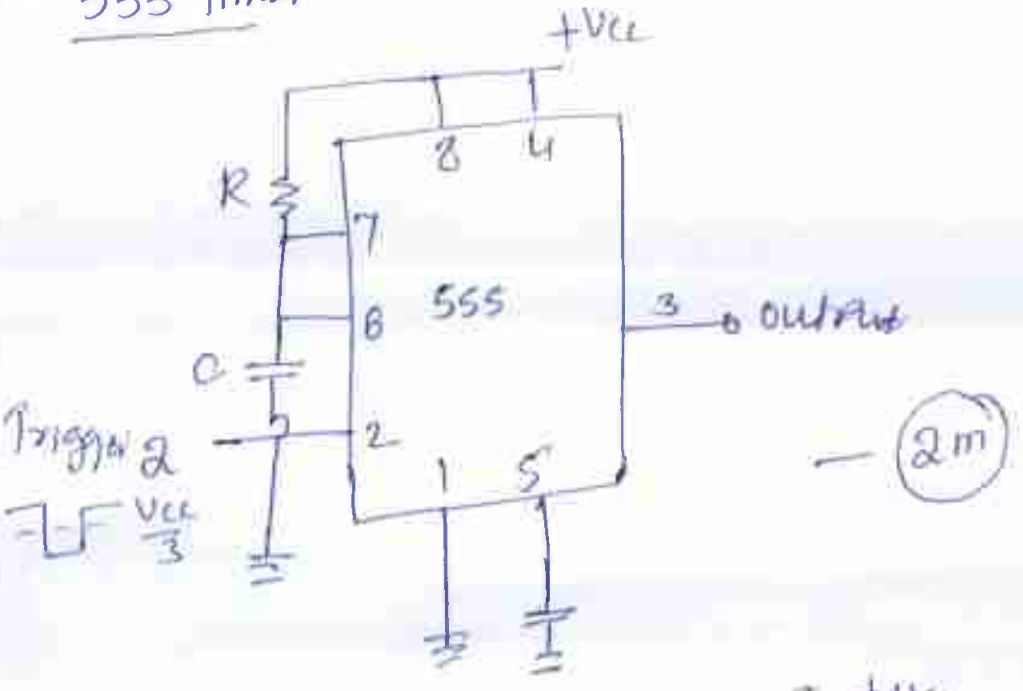
Explanation each Pin and Blocks ~~each~~ 4m

1 555 Timer Consists of two comparator and voltage divider Consists of 3 equal resistance Due to voltage divider the voltage of non inverting Comparator 2 is fixed at $\frac{V_{cc}}{3}$ the comparator 2 output goes high this output is given to reset input RS FF high output.

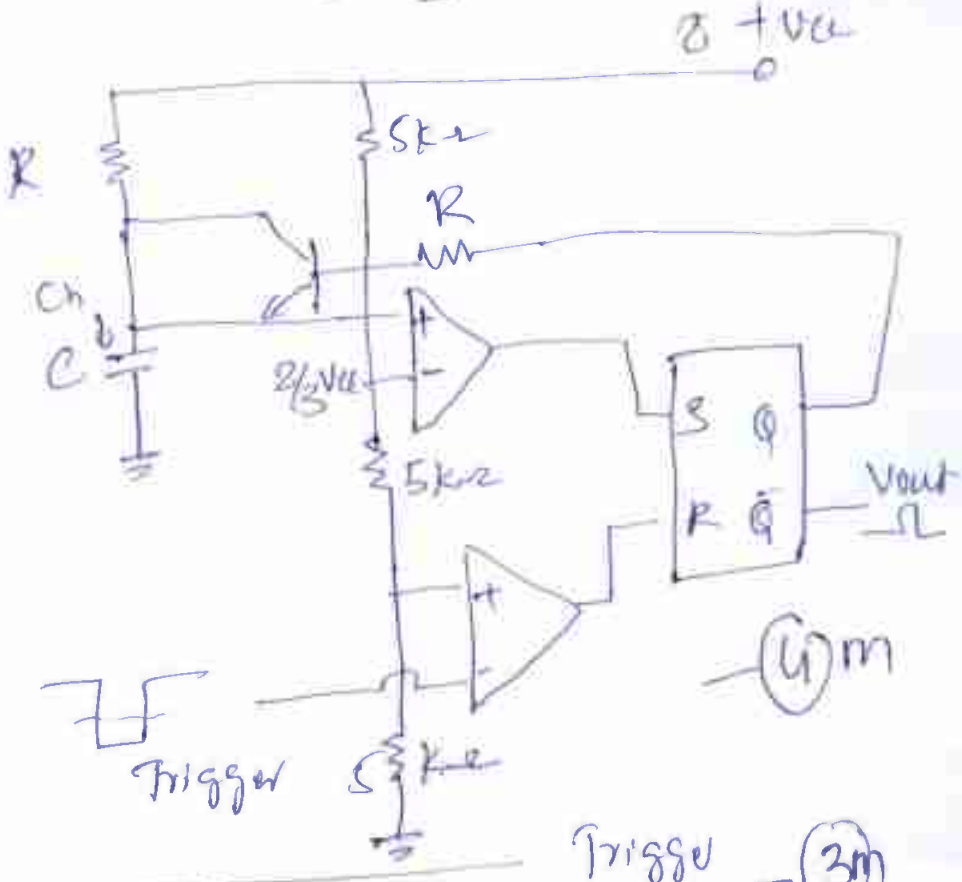
Subject Title :

Subject Code : 18EE46

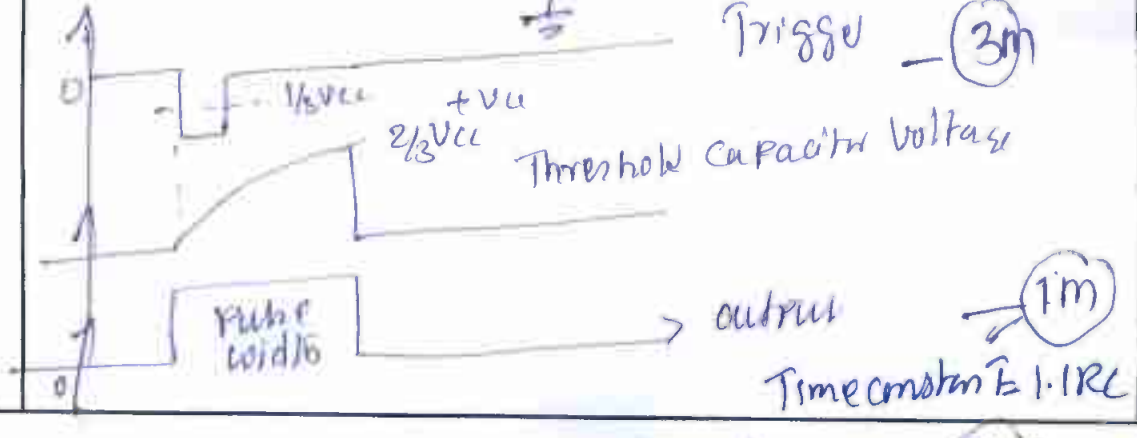
Question Number	Solution	Marks Allocated
10(a)	monoStable Operation 555 Timer	12m.



— (2m)



(4)m



(3m)

(1m)

Time constant = 1.1RC

Operation — (2m)

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Subject Title : Subject Code : 18EE46

Question Number	Solution	Marks Allocated
10.b	(i) Lock range : When PLL is in Lock, it can track frequency changes in the incoming Signal. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock range. — (2M) (ii) Capture range : The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. it is also expressed as % of f_o — (2M) (iii) Pull in Time : The capture of an input signal does not take place as soon as the signal is applied but it takes finite time The total time taken by the PLL to establish lock is called Pull in time. — (2M) (iv) Tracking Range : the range of frequencies over which PLL will track the input frequency signal and remains locked is referred as PLL lock range. the lock range is usually band of frequencies above and below the PLL free running frequency as described. — (2M)	8M.

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