CBCS SCHEME

18EC72

Seventh Semester B.E. Degree Examination, Jan./Feb. 2023
VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With neat graph define Moore's law. Explain the history of integrated structures. **(06 Marks)**

b. Realize CMOS logic structure for the Boolean expressions :

i) $y = \overline{(a \cdot b) + (c \cdot d)}$ ii) $y = a \cdot (b + c)$. **(06 Marks)**

c. With neat diagrams, explain 3 regions of operations of nMOS transistor. **(08 Marks)**

OR

2 a. List the any three non ideal features of transistors. Explain each in detail. **(06 Marks)**

b. Draw the diagram of general logic gate structure. Explain 2-input CMOS NAND gate functioning using truth table. **(06 Marks)**

c. Draw schematic diagram of CMOS inverter. Explain the graphical derivation of CMOS inverter DC characteristics. **(08 Marks)**

Module-2

3 a. With neat diagrams, explain the complete CMOS fabrication process. **(12 Marks)**

b. Using relevant equations explain full scaling (constant field scaling) applied to i) Channel length ii) Channel depth iii) Oxide thickness iv) Junction depth v) Supply vi) Threshold voltage vii) Doping densities N_A, N_D. **(08 Marks)**

OR

4 a. Write a short note on timing analyzer. **(06 Marks)**

b. With neat diagrams, explain the lumped representation of parasitic MOSFET capacitances. **(08 Marks)**

c. Draw and explain layout rules for transistors. **(06 Marks)**

Module-3

5 a. Explain various stages of timing optimization in VLSI design. **(08 Marks)**

b. With equations explain the calculation of inverter delay. **(06 Marks)**

c. Estimate the propagation delay t_{pd} for unit inverter driving 'm' identical unit inverters using Elmore delay. **(06 Marks)**

OR

6 a. Draw the diagram of photo masking with a negative resist and explain. **(08 Marks)**

b. What is logical effort? Explain HI-Skew inverter construction by down sizing of nMOS transistor. **(06 Marks)**

c. Explain pseudo nMOS inverter with schematic diagram and DC transfer characteristics. **(06 Marks)**

Module-4

7 a. Draw and explain the functioning of pulse generators. (08 Marks)
b. Explain the working of resettable flip-flops and latches. (12 Marks)

OR

8 a. Draw and explain the features of C^2MOS latch. (08 Marks)
b. With neat circuit diagrams, explain 4 transparent latches. Write the advantage and disadvantage of each. (12 Marks)

Module-5

9 a. Draw the diagram of 4 bit × 4 bit NOR based ROM array, explain the functioning. (08 Marks)
b. What is static RAM? With neat diagram explain any 3 static RAM circuits. (12 Marks)

OR

10 a. Write a short note on design for testability. (06 Marks)
b. Explain manufacturing test principles in detail. (06 Marks)
c. Explain the logic verification principles. (08 Marks)

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