CBCS SCHEME

USN | | | | | | | | | | |

15TE73

Seventh Semester B.E. Degree Examination, Jan./Feb. 2023
CMOS VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the NMOS enhancement mode transistor operation for different values of V_{GS} and V_{OS}. **(08 Marks)**

b. Explain the CMOS inverter transfer characteristics highlighting the regions of operations of the MOS transistor. **(08 Marks)**

OR

2 a. With neat sketch, explain the CMOS p – well process steps to fabricate a CMOS inverter. **(12 Marks)**

b. Compare CMOS and Bipolar transistor. **(04 Marks)**

Module-2

3 a. With a neat diagram, explain λ based design rules for wired (nMOS and CMOS). **(08 Marks)**

b. Draw the NMOS circuit diagram and stick diagram for the nMOS implementation of the Boolean expression $y = \overline{AB + CD}$. **(08 Marks)**

OR

4 a. Derive the expression for sheet resistance R_S. **(06 Marks)**

b. Derive an expression for the estimation of CMOS inverter delay. **(10 Marks)**

Module-3

5 a. Derive the scaling factor for :
i) Saturation current
ii) Current density
iii) Power dissipation/unit area
iv) Maximum operation frequency. **(08 Marks)**

b. Explain the General arrangement of 4 bit ALU. **(08 Marks)**

OR

6 a. With a neat diagram, explain 4 × 4 Based shifter. **(08 Marks)**

b. Explain Manchester Career's chain circuit. **(08 Marks)**

Module-4

7 a. Discuss the architectural issues related to sub-system design. **(08 Marks)**

b. Explain the structured design approach for the implementation of a parity generator with relevant stick diagram. **(08 Marks)**

OR

8 a. Explain switch logic implementation of a 4 × 4 four way multiplexer. **(08 Marks)**

b. Write short notes on FPGA architecture with a diagram. **(08 Marks)**

Module-5

9 a. Explain 3-transitor dynamic RAM-cell. **(08 Marks)**

b. Explain write operation, read operation for four transistor dynamic and six transistor static CMOS memory cell. **(08 Marks)**

OR

10 a. List the system Timing Considerations. **(08 Marks)**

b. Write short notes on Built in Self Test (BIST). **(08 Marks)**

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