USN

CMRIT

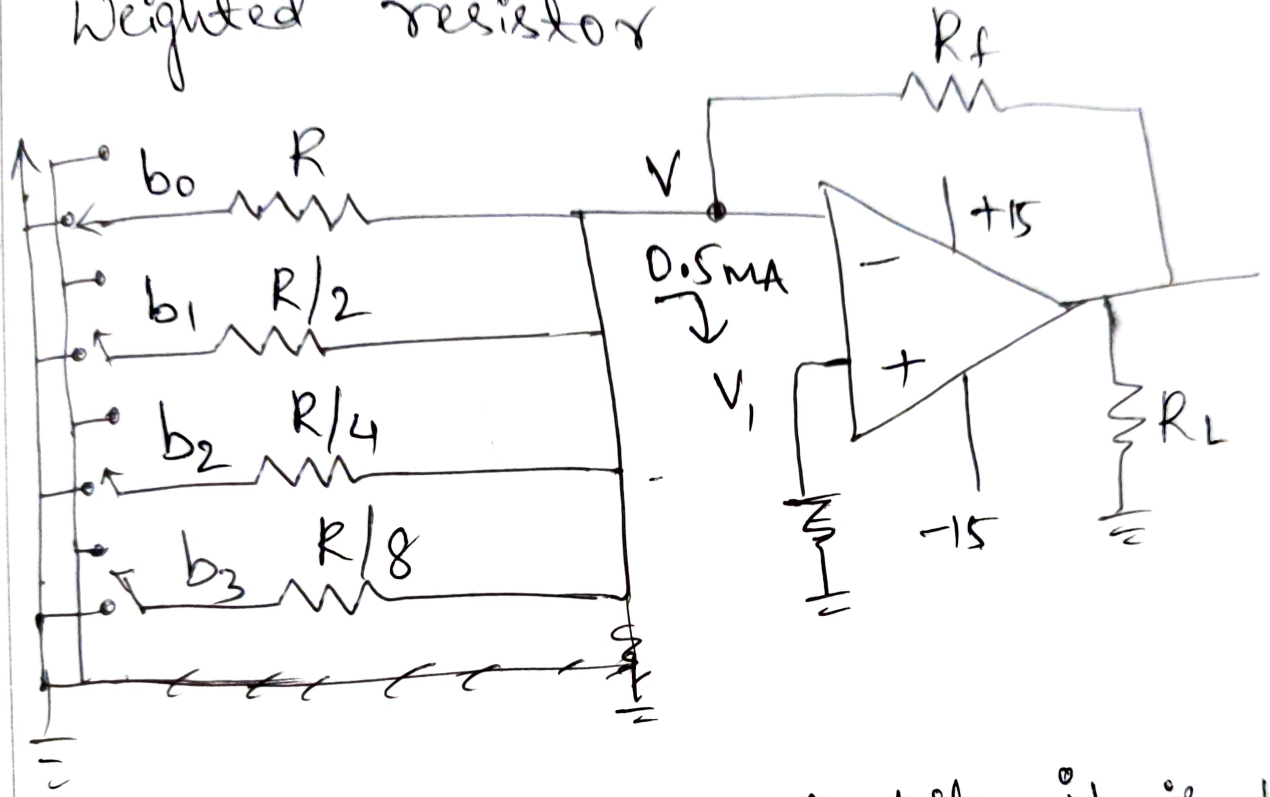
Internal Assessment Test III– August 2022

Sub:	Analog Circuits					Sub Code:	18EC42	Branch :	ECE
Date:	26-08-2022	Duration:	1.5 hour	Max Marks:	50	Sem/Sec :	4th sem /A,B,C,D		OBE

ANSWER ANY 5 FULL QUESTIONS

		MARKS	CO	RBT
1.	With circuit diagram and waveforms, explain the working of binary weighted resistor 4 bit Digital to Analog converter.	[10]	CO4	L2
2.	Explain the working of a monostable multivibrator using 555 Timer IC. Design a circuit using 555 Timer to get a monoshot pulse of width 10ms. Choose C = 1μF	[10]	CO5	L3
3.	Explain the operation of 4-bit R-2R DAC with neat circuit. For the R-2R DAC, with R=10kΩ and RF=20kΩ and V_{REF}=5V, determine the output voltage when the inputs b0=b1=5V and b2=b3=0V	[10]	CO4	L3
4.	Explain the operation of a Successive -approximation ADC with neat circuit diagram.	[10]	CO4	L2
5.	Draw the circuit and frequency response of a first order low pass filter. Design a first order low pass filter to have a cutoff frequency of 1kHz with a passband gain of 2.	[10]	CO4	L2
6.	With necessary circuit and waveforms, explain the operation of a Astable multivibrator (Symmetric and Asymmetric) using 555 timer IC.	[10]	CO5	L2
7.	With a neat block diagram explain the working of a Voltage series feedback amplifier. Derive an expression for the overall gain, input and output impedances.	.[10]	CO2	L3
8.	Draw the circuit and frequency response of a first order high pass filter. Design a first order high pass filter to have a cutoff frequency of 1kHz with a passband gain of 2.	[10]	CO4	L2
9.	Give the circuit diagram, gain expression and frequency response plots of:- (a) First order Low pass filter (b) Second order Low pass filter (c) Wide band pass filter (d) Narrow band reject filter	[10]	CO4	L2
10	Explain the working of positive and negative half wave precision rectifier with necessary circuit and wave forms.	[10]	CO4	L2

1) Weighted resistor



* Since there are 4 input bits it is known as 4-bit DAC.

* If $R = 10\,k\Omega$, $\frac{R}{2} = \frac{10}{2} = 5\,k\Omega$

$\frac{R}{4} = \frac{10}{4} = 2.5\,k\Omega$, $\frac{R}{8} = \frac{10}{8} = 1.25\,k\Omega$

* Let us consider if the switch b_0 is closed & connected to 5V V_{cc} and the remaining switches are open.

i.e $\Rightarrow$ $b_0 = 1$, $b_1 = b_2 = b_3 = 0$.

* Then the current is given as $I = \frac{V}{R}$

$$I = \frac{5}{10} = 0.5\,mA.$$

This is the ~~a~~ current across R and for the ideal one the current across R_f is same as that of 0.5 mA

* ~~Th~~ Since all ~~th~~ other switches are grounded the current through them is zero.

* The total current through R_f is given as

$$I_f = (0.5 + 0 + 0 + 0)\,mA$$
$$= 0.5\,mA.$$

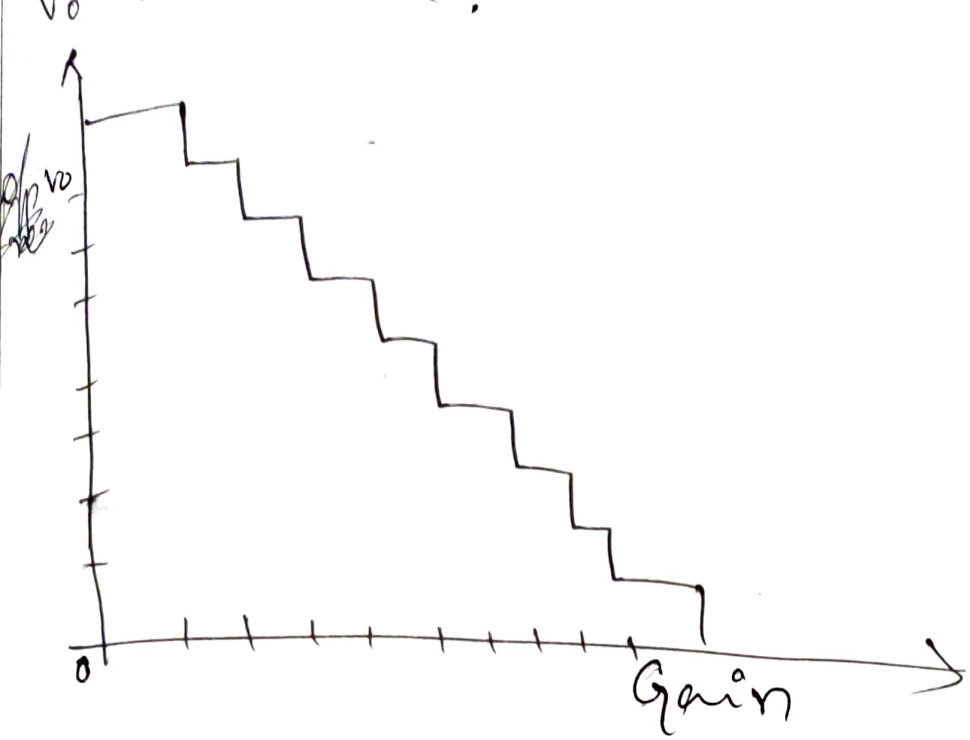
* Therefore the o/p voltage is given as

$$V = IR = (0.5)(10) = 5\,V.$$

* The maximum voltage is obtained when all the switches are closed.

$$V_0 = -R_f \left[\frac{R}{2^0} + \frac{2R_f}{2R} + \frac{5}{R} + \frac{5}{2R/2} + \frac{5}{R/4} + \frac{5}{R/8} \right]$$

$$= -1k \left[\frac{5}{10} + \frac{5}{5} + \frac{5}{2.5} + \frac{5}{1.25} \right]$$



The main drawback of this type DAC is that the 8 different resistance values. which may not be available.

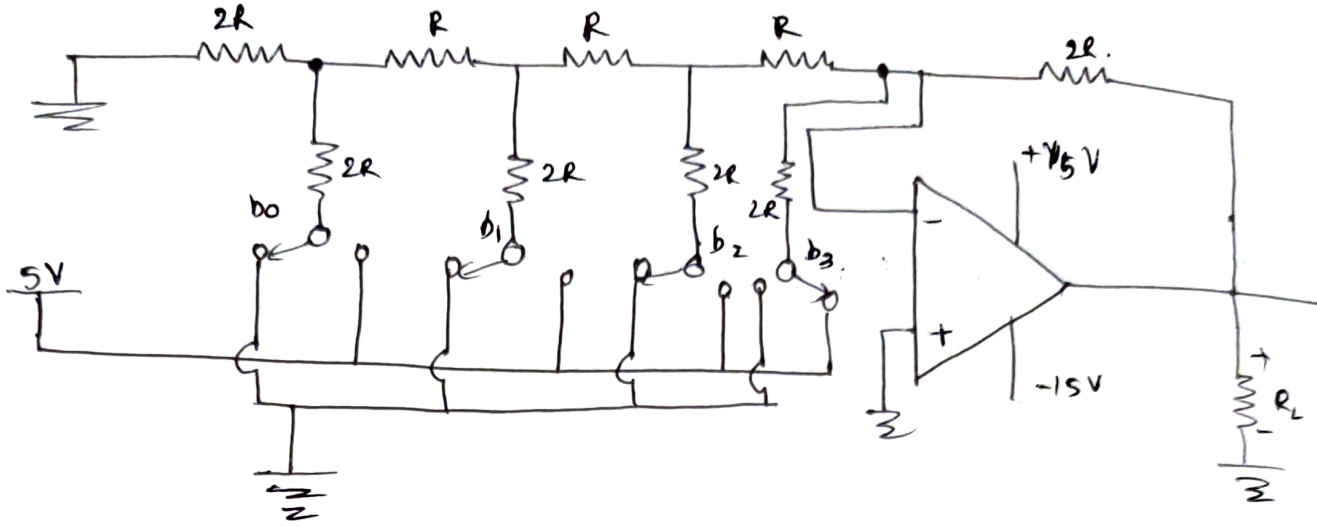
$$V_o = -R_f \left[R + 2R + 4R + 8R \right]$$

Due to this drawback we have arrived at R-2R ladder type.

The current calculated based on the switch position will be the current flowing through the feedback resistor R_f.

Weighted ~~Ckts~~ resistor DAC

3.



* 4-bit R-2R DAC is used instead of binary weighted re because in the binary weighted resistor there is a requiren of weighted resistors which are not always available.

* In this R to 2R ladder we use

$R = 10k\Omega$

$2R = 20k\Omega$

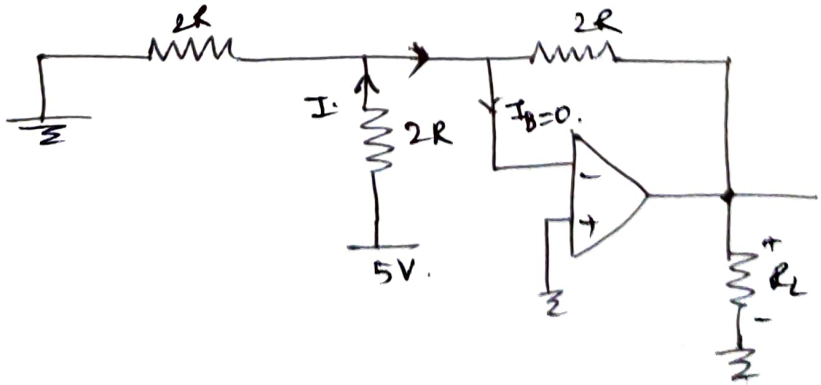
$R_f = 20k\Omega$ Resistor which are easily ava

* b_0 is LSB & b_3 is MSB.

b_0 towards the left end and b_3 towards the Right are bits.

* According to the above circuit lets consider b_3 pin to be connected to the 5V pin.

Hence,



On Applying thevenins theorem, we get

$$R_{th} = \{(((2R \| 2R + R) \| 2R) + R) \| 2R) + R\}$$

$$R_{th} = 2R$$

$$= R_f$$

$$I = \frac{V}{R}$$

$$= \frac{5}{20K}$$

$$= 0.25\,mA$$

$$V_o = -0.25\,mA \times 20K$$

$$= -5V.$$

The Output of the R-2R ladder is given by.

$$V_o = -V_{ref} R_f \left[\frac{b_0}{16R} + \frac{b_1}{8R} + \frac{b_2}{4R} + \frac{b_3}{2R}\right]$$

$20 \times 10^3 \left[\frac{5}{2 \times 10}\right.$

The Output of the DAC is Maximum when all the bits are high

$$V_o = -20 \times 10^3 \left[\frac{5}{16R} + \frac{5}{8R} + \frac{5}{4R} + \frac{5}{2R}\right]$$

$$= -\frac{20 \times 10^3}{10^3} \left[\frac{5}{16} + \frac{5}{8} + \frac{5}{4} + \frac{5}{2}\right]$$

$$V_o = -9.37\,V$$

for $R = 10K\Omega$

$R_f = 20K\Omega$

$V_{ref} = 5V$

when $b_0 = b_1 = 5V$ & $b_2 = b_3 = 0V$.

$$V_o = -5 \times \frac{20 \times 10^3}{10^3} \left[\frac{1}{160} + \frac{1}{80} + \frac{0}{40} + \frac{0}{20}\right]$$

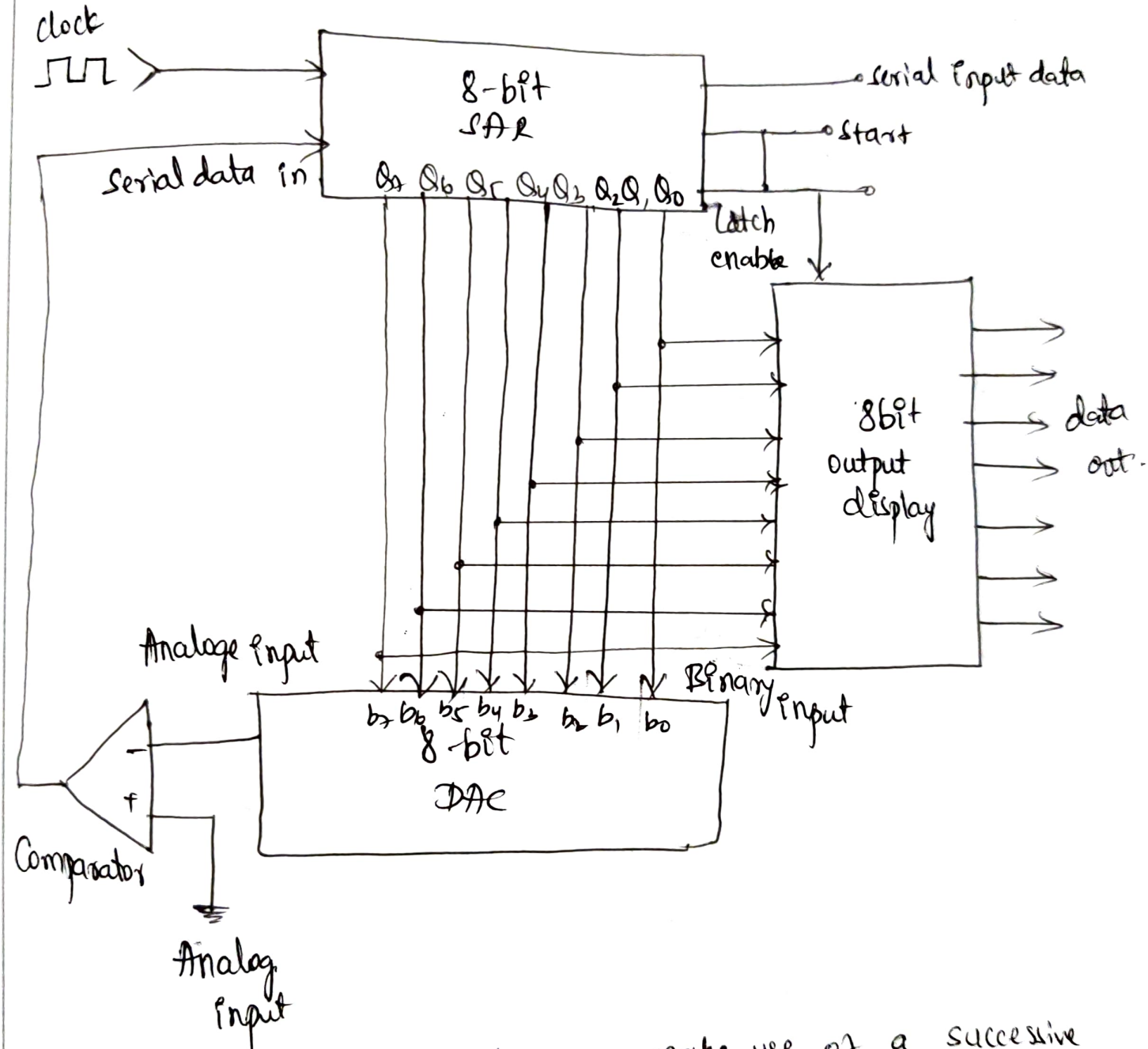
$$= -5 \times 2 \left[\frac{1}{16} + \frac{1}{8}\right]$$

(4)

Successive approximation ADC

ADC - Analog to digital converter.

The below is the successive approximation type ADC.



* In successive approximation we make use of a successive approximation register, a comparator, clock pulse etc.

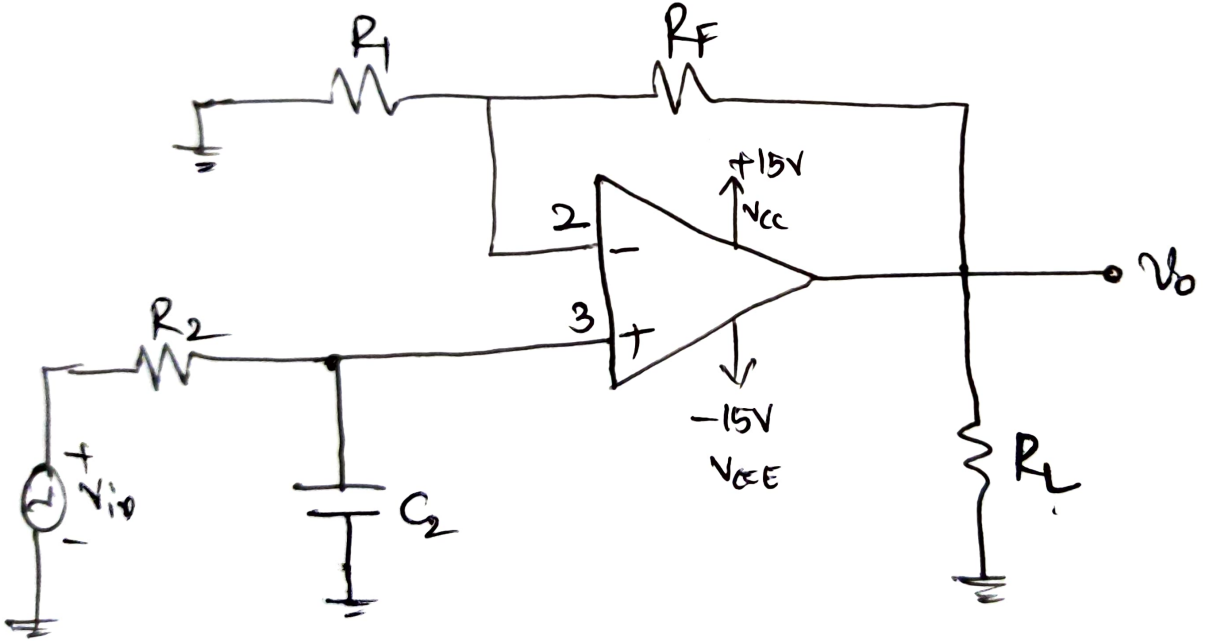
* When the MSB bit Q_7 is made low to high of SAR signal the Q_7 is pushed up. and there is a start of comparator cycle

* If the comparator output is low, then the bit
then Q_6 is made to accept.
* If comparator output is high, then the bit
bit Q_7 is set and not moved anywhere.
* Then next considering Q_6, based on the
value and DAC output value Q_6 is either set or
* Similary all the bits from MSB to LSB
processed based on the comparator values.
* Finally when Q_0 is tried, the SAR forces a
then the process stops.
* Finally the output is seen through
* The successive approximation ADC
format or one after the other format.
bit of SAR.

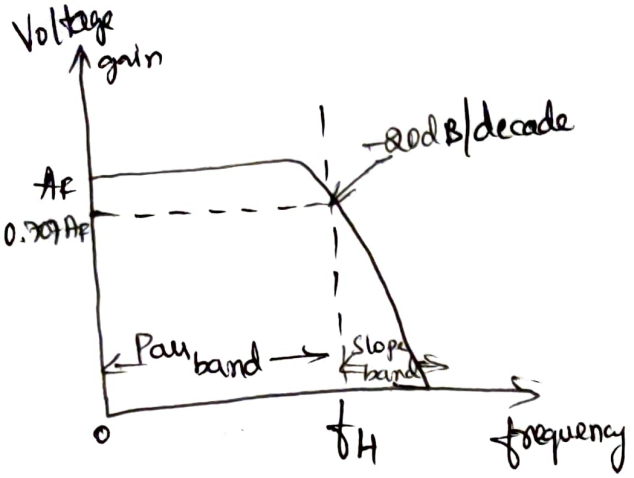
bits of SAR.

First order low pass butterworth filter.

* First order low pass filter is designed using RC c



Frequency response :



By applying voltage divider rule to the circuit, we get

$$V_1 = \frac{-jX_C}{R - jX_C} V_{in} \quad \text{—(1)}$$

$$j = \sqrt{-1}, \quad -jX_C = \frac{1}{j2\pi f_H C}$$

eq" (1) $\Rightarrow$

$$V_1 = \frac{\frac{1}{j2\pi f_H C}}{R + \frac{1}{j2\pi f_H C}} V_{in}$$

$$V_1 = \frac{1}{1 + j2\pi f_H RC} V_{in} \quad \text{—(2)}$$

W.K.T

$$V_o = A_F V_1$$

$$V_o = \left(1 + \frac{R_F}{R_1}\right) \frac{V_{in}}{1 + j2\pi f_H RC}$$

$$\boxed{\frac{V_o}{V_{in}} = \frac{A_F}{1 + j2\pi f_H RC}} \quad \text{—(3)}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{1 + j(f/f_H)}$$

Magnitude $\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}}$

Phase angle $\phi = \tan^{-1}\left(\frac{f}{f_H}\right)$

Given: $f_H = 1\,kHz$

$$R = \frac{1}{2\pi f_H C}$$

$$R = \frac{1}{2(\pi)(1\times10^{3})(\quad\times10^{-6})}$$ { considering $C = 1\mu F$ }

$$R = 0.1591\,\Omega \times 1000$$

$$R = 159.1\,\Omega$$

Gain $= 2 = A_F$

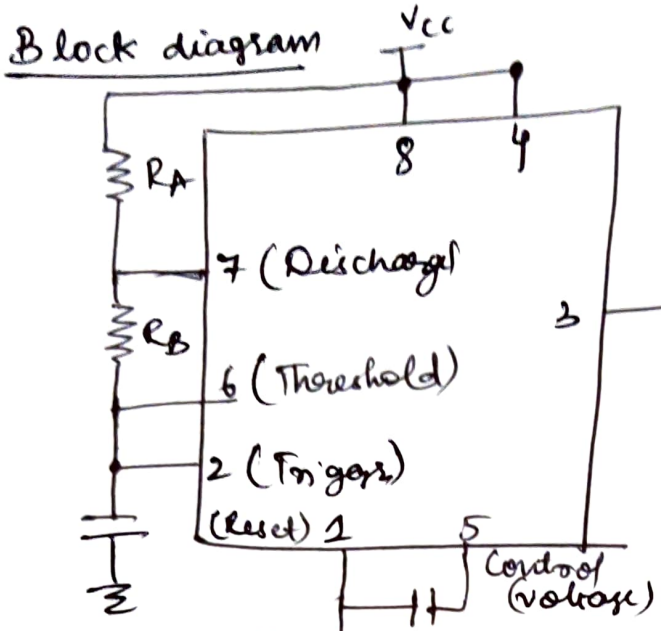
$$2 = 1 + \frac{R_F}{R_1}$$

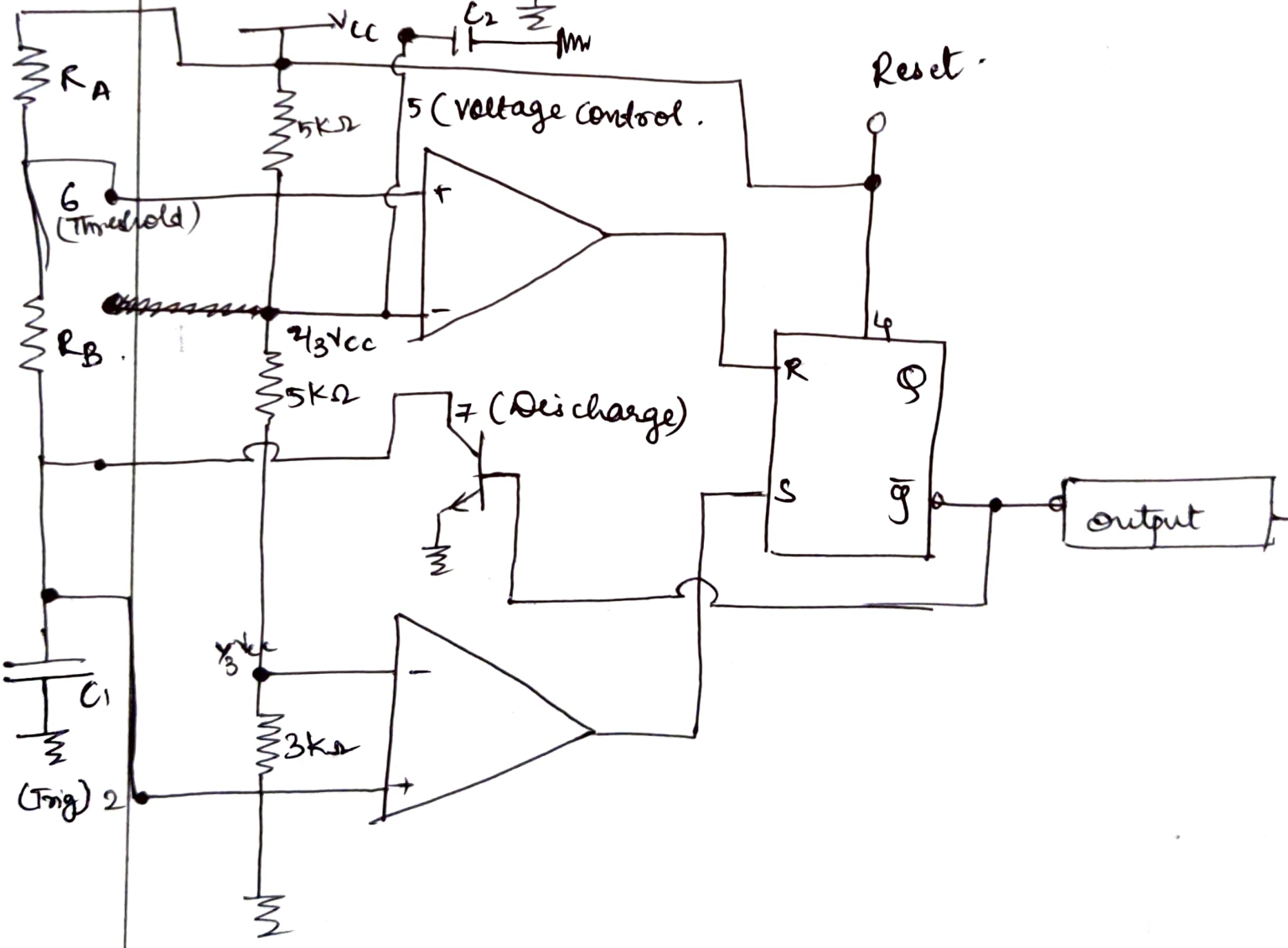
This is possible only when $R_F = R_1$

$$\therefore R_F = R_1 = 10k\Omega$$

$R_f = R_1 = 10K\Omega$

6. Block diagram





Astable Multivibrator

The both the states are not stable in a Astable Multivibrator.

(1) when the Astable Multivibration is power on or switched on for the first.

upper comparator is low $R = 0$

lower comparator is high $S = 1$

hence the flipflop is set $Q = 1$ & $\bar{Q} = 0$ the transistor behaves as a open circuit and the capacitor starts charging through the R_A & R_B resistors.

(2) when the capacitor voltage is more than $\frac{1}{3} V_{cc}$ then the

upper comparator is low $R = 0$

low comparator is Low $S = 0$.

when $S = 0; R = 0$ the flipflop is memory state hence it function same as $S = 1$ & $R = 0$ the above state where capacitor is charging

(3) when the capacitor voltage is more than $\frac{2}{3} V_{cc}$ then the

upper comparator is high $R = 1$

lower comparator is low $S = 0$

hence the flipflop is in reset state $Q = 0$ & $\bar{Q} = 1$ here the transistor acts as a closed switch and the capacitor begin to discharge.

when capacitor discharges $S = 0$, $R = 0$ at this time the flipflop is in memory state & hence discharges

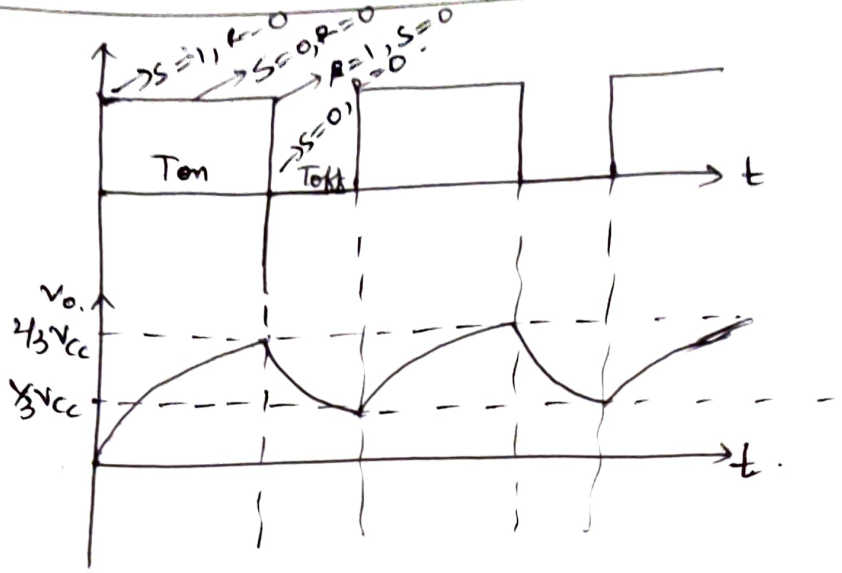
(4) when the capacitor voltage goes below $\frac{1}{3} V_{cc}$ then the

upper comparator is low $R = 0$

lower compabator is high $S = 1$

The transistor switch acts as open switch and the

Process starts to repeat.



To find the Ton & Toff.

$$V_c(t) = V_{final} + (V_{initial} - V_{final}) e^{-T/RC}$$

for Ton

$$V_c(t) = V_{cc} + (\tfrac{1}{3}V_{cc} - V_{cc}) e^{-Ton/RC}$$

$$\frac{2}{3}V_{cc} = V_{cc} + (\tfrac{1}{3}V_{cc} - V_{cc}) e^{-Ton/RC}$$

$$\frac{2}{3} - 1 = \left(\frac{1}{3} - 1\right) e^{-Ton/RC}$$

$$-\frac{1}{3} = -\frac{2}{3} e^{-Ton/RC}$$ here, $R = R_A + R_B$.

$$-\ln(2) = -Ton/RC$$

$$0.693 (R_A + R_B) C = Ton$$

for Toff

$$\tfrac{1}{3}V_{cc} = 0 + (0 - \tfrac{2}{3}V_{cc}) e^{-Toff/R_BC}.$$

$$-\frac{Toff}{R_BC} = \ln(1/2)$$

$$Toff = 0.693 R_B C$$

$$T = T_{on} + T_{off}$$

$$= 0.693\, C\, (R_A + 2R_B)$$

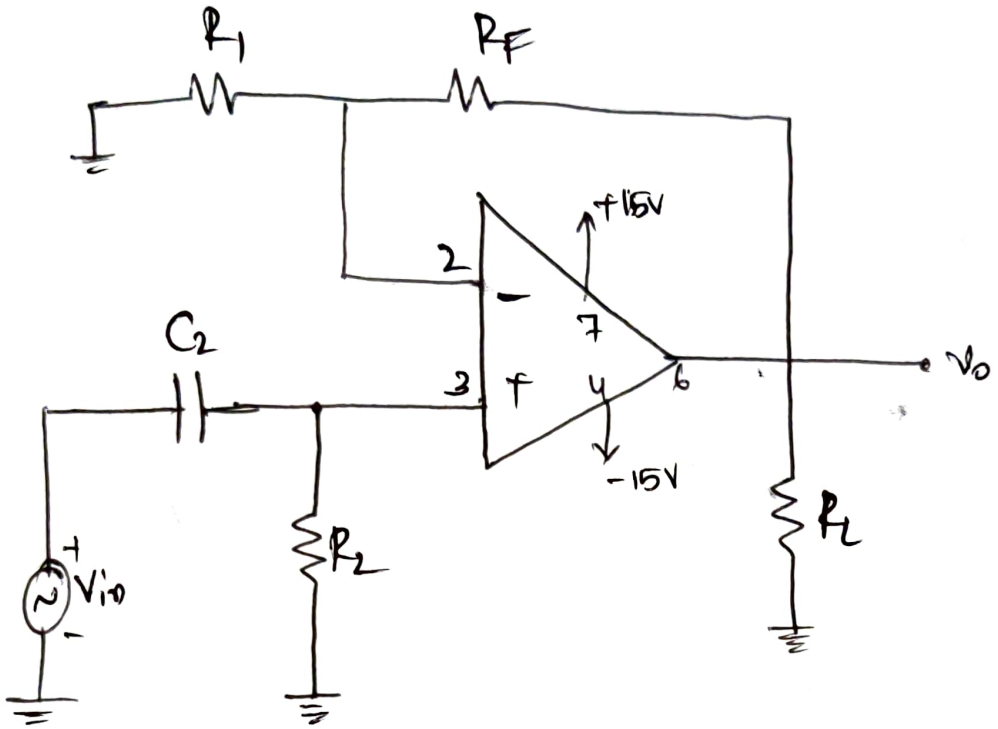
Duty cycle

- Duty cycle $= \dfrac{T_{on}}{T} \times 100.$

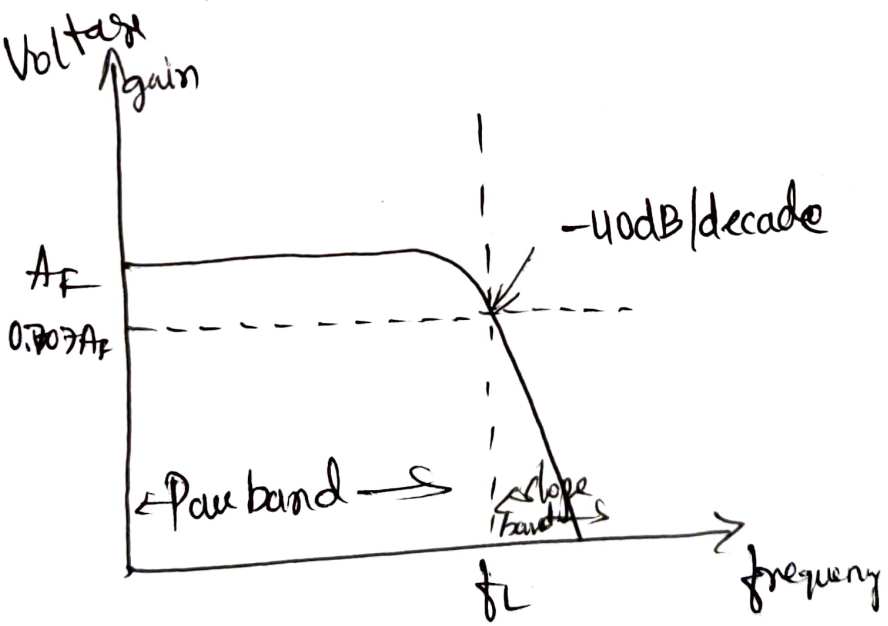
$$= \frac{0.693\,(R_A + R_B)\,C}{0.693\,(R_A + 2R_B)\,C} \times 100.$$

$$= \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

(8) First order high pass butterworth filter



Frequency response:



By applying voltage divider rule to the circuit, we get

$$V_1 = \frac{R}{R - jX_C} V_{in}$$

$$V_1 = \frac{R}{R + \frac{1}{j2\pi f_L C}} V_{in}$$

$$V_1 = \frac{j2\pi f_L RC}{1 + j2\pi f_L RC} V_{in} \quad \text{— (1)}$$

$$V_o = A_F V_1$$

$$V_o = \left(1 + \frac{R_F}{R_1}\right) \frac{j2\pi f_L RC}{1 + j2\pi f_L RC} V_{in}$$

$$\frac{V_o}{V_{in}} = \frac{(A_F)\, j2\pi f_L RC}{1 + j2\pi f_L RC}$$

$$\boxed{\frac{V_o}{V_{in}} = \frac{A_F j(f/f_L)}{1 + j(f/f_L)}}$$

$$\text{Magnitude } \left|\frac{V_o}{V_{in}}\right| = \frac{A_F (f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

$f_L = 1\,KHz$, $C = 0.01\,\mu F$,

$$R = \frac{1}{2\pi f_L C}$$

$$R = \frac{1}{2 \times \pi \times 1 \times 10^3 \times 10^{-6} \times 1}$$

$R = 159.1\,\Omega$

$A_F = 2$

$1 + \frac{R_F}{R_1} = 2$

let $R_F = R_1$

only then $A_F = 2$

New $R_F = R_1 = 10k\,\Omega$

$$\frac{V_o}{V_{in}} = \frac{2\,j(f/10^3)}{1 + j(f/10^3)}$$

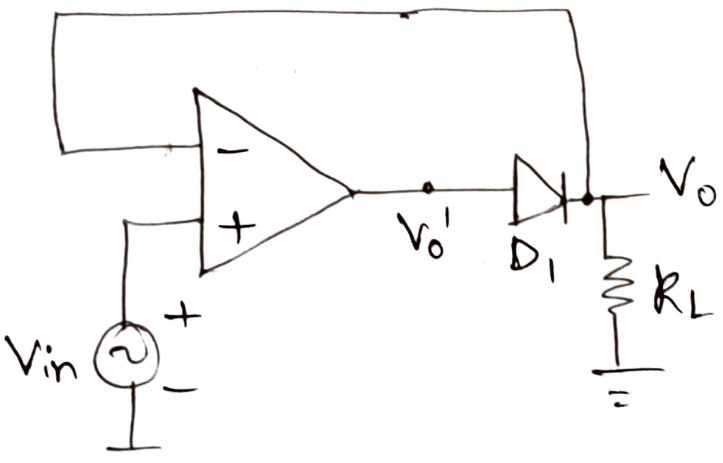
10) Precision Rectifier

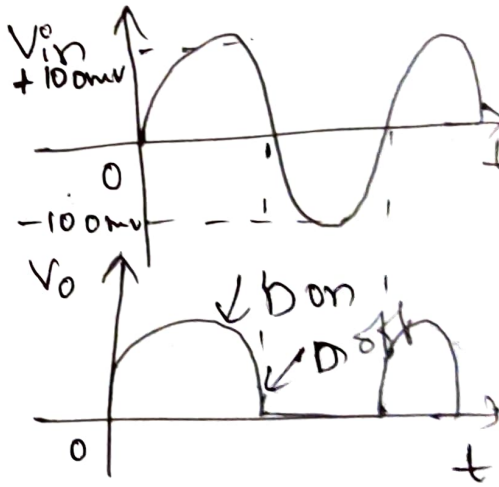
Normally diodes required the input to be more than the ideal value. So for precision rectifier which is a combination of op-amp and diodes effective voltage is reduced by gain. The effective voltage is given as

$$V_{r_{eff}} = \frac{V_r}{A}$$

Precision Half wave Rectifier

Positive Half wave Rectifier.



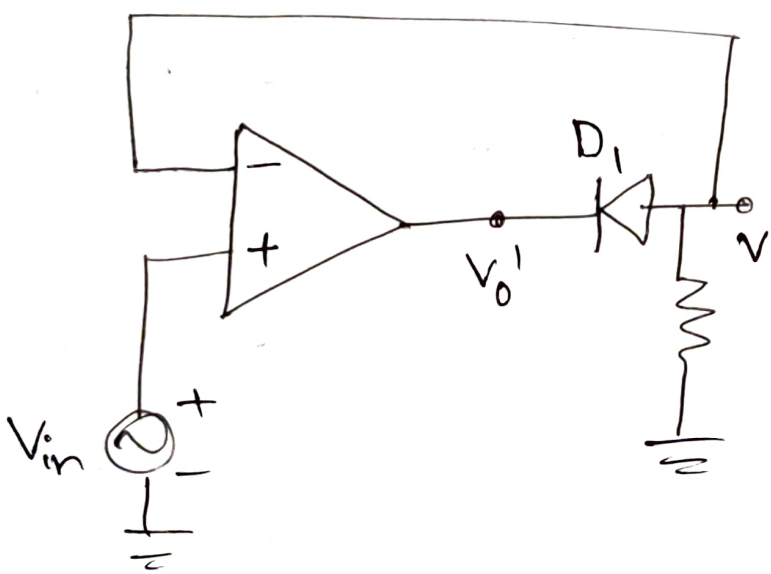


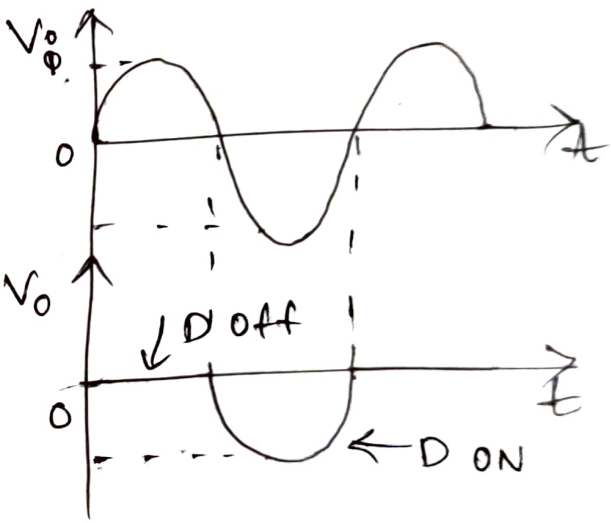
* The op-amp is made to work as voltage follower The combination of op-amp and diode is used.
* When the positive voltage is given or when the voltage is increased positive the voltage V_o' also increases which makes the diode forward biased and the Diode is ~~on~~ in 'ON' condition as shown in the graph.

* When the voltage increases negatively then the diode is reverse biased even when V_o' is increased. This makes the diode D_1 off during the negative half cycle as shown in the diagram:

* When V_o' increases during positive half cycle the circuit acts as a voltage follower and the output follows the input.

Negative half cycle





During the negative half cycle

* The negative half cycle design is same as that of positive half cycle only change is that the diode direction is reversed.

* When the voltage is increased positively the

diode D_1 is reverse biased even when the V_o is increased therefore the output voltage is zero, as shown in the graph.

When the negative voltage is applied or when the ~~-ve~~ voltage is increased negatively the diode D_1 is forward biased with the voltage V_o' increased. The output voltage follows the input voltage during the negative half cycle as shown in the graph.