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Internal Assessment Test 1 – Dec 2022

Sub:	Analog and Digital Electronics					Sub Code:	21CS33	Branch:	CSE
Date:	1/12/22	Duration:	90 mins	Max Marks:	50	Sem / Sec:	3rd semester/A,B,C		OBE

	Answer any FIVE FULL Questions	MARKS	CO	RBT
1	A switching circuit has 2 control inputs C1 and C2, two data inputs X1 and X2, and one output Z. The circuit performs one of the logic operations: NAND, NOR, XOR and EQU(Equivalence) on the two data inputs. The function performed depends on the control inputs (a) Derive a truth table for *Z*. (b) Use a Karnaugh map to find a minimum AND-OR gate circuit to realize *Z* (c).Implement using NAND Gates		CO2	L2,L3

Solution:

Truth Table

	C1	C2	X1	X2	Y
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	0
12	1	1	0	0	1
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	1

SUM of PRODUCTS

Map

	X1'X2'	X1'X2	X1X2	X1X2'
C1'C2'	1	1	0	1
C1'C2	1	0	0	0
C1C2	1	0	1	0
C1C2'	0	1	0	1

Map Layout

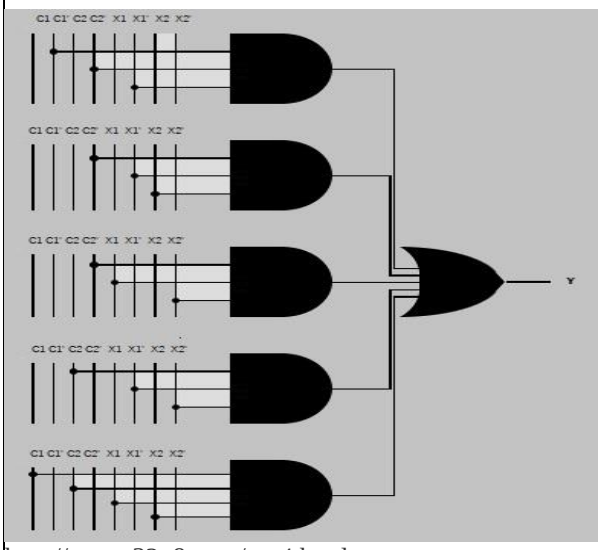
	X1'X2'	X1'X2	X1X2	X1X2'
C1'C2'	0	1	3	2
C1'C2	4	5	7	6
C1C2	12	13	15	14
C1C2'	8	9	11	10

Groups

(0,1)	C1'C2'X2
(1,9)	C1'X1'X2
(2,10)	C1'X1X2'
(4,12)	C2X1'X2'
(15)	C1C2X1X2

Y= C1'C2'X2 + C1'X1'X2 + C1'X1X2' + C2X1'X2' + C1C2X1X2

Implementation using NAND gate

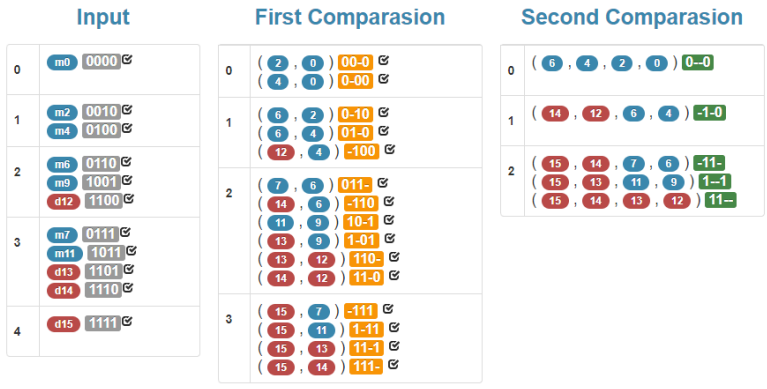


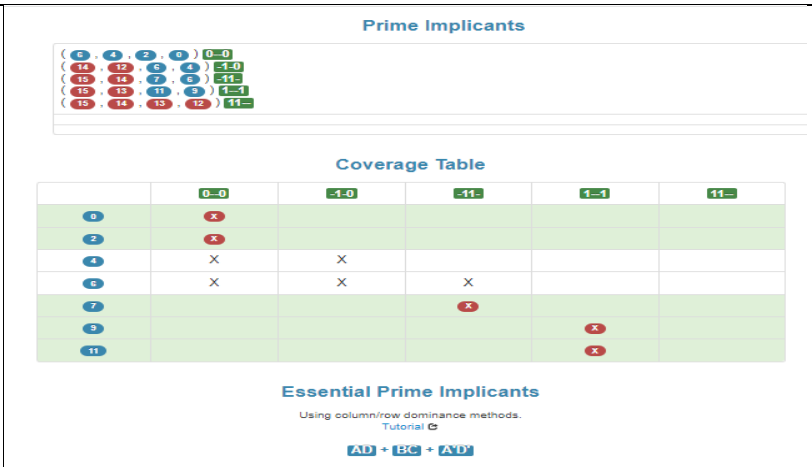
http://www.32x8.com/var4.html

2 A Digital system is to be designed in which month of the year is given as input is four bit form. The month January is represented as "0000", February as "0001" and so on. The output of the system is 1 corresponding to the input of the month containing 31 days or otherwise is 0 consider excess number in the input beyond '1011' as don't cares conditions. [10] CO2 L2,L3

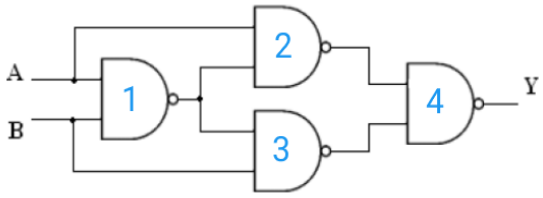
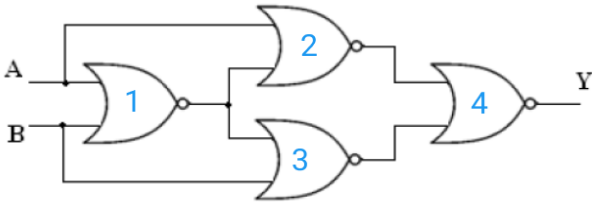
(a) Write truth table ,SOP
(b) Simplify for SOP using **QM method**
(c) Realize using Basic Gates

Solution :





http://quinemccluskey.com/?min=0%0D%0A2%0D%0A4%0D%0A6+%0D%0A7%0D%0A9%0D%0A11&dont=

3 (a)	Define 1.Implicant 2.Prime Implicant 3.Essential Prime Implicant 4. Selective prime implicant 5.Redundant prime implicant **Solution:**	[05]	CO2	L1,L2
(b)	Design function EX OR gate 1) using NAND gate only 2) using NOR gate only (e) Ex-OR gate: $Y = A \oplus B$  A B Y: 0 0 0; 0 1 1; 1 0 1; 1 1 0 (e) Ex-NOR gate: $Y = A \odot B = (A \oplus B)'$  0 0 1; 0 1 0; 1 0 0; 1 1 1	[05]	CO2	L1,L2

4(a)	Using the method of map-entered variables, use four-variable maps to find a minimum sum-of-products expression for $F(A, B, C, D, E) = m(0, 2, 5, 8, 9) + d(6, 10) + E(m7, m12)$ where the m's represent minterms of the variables A, B, C, and D.	[06]	CO2	L2,L3

Truth Table

	A	B	C	D	Y
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	X
7	0	1	1	1	E
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	X
11	1	0	1	1	0
12	1	1	0	0	E
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	0

Map

	C'D'	C'D	CD	CD'
A'B'	1	0	0	1
A'B	1	1	E	X
AB	E	0	0	0
AB'	1	1	0	X

Map Layout

	C'D'	C'D	CD	CD'
A'B'	0	1	3	2
A'B	4	5	7	6
AB	12	13	15	14
AB'	8	9	11	10

Step 1 : consider 1s and don't cares and E=0

	C'D'	C'D	CD	CD'
A'B'	1	0	0	1

A'B	1	1	0	X
AB	0	0	0	0
AB'	1	1	0	X

Groups

(0,2,8,10)	B'D'
(8,9)	AB'C'
(5)	ABC'D

SO MS1=B'D'+AB'C'+ABC'D

STEP 2 : consider variable E = 1 and make all 1s don't care and consider all don't care

	C'D'	C'D	CD	CD'
A'B'	X	0	0	X
A'B	X	X	1	X
AB	1	0	0	0
AB'	X	X	0	X

Groups

(5,7)	A'BD
(8,12)	AC'D'

SO MS2= (A'BD +AC'D')E =A'BDE +AC'D'E
SO minimum SOP Boolean expression is =MS1+MS2= B'D'+AB'C'+ABC'D+ A'BDE +AC'D'E

4(b) What are the benefits of MEV over KM Method. [04] CO2 L1,L2

Solution:
K-map is the best manual technique to solve Boolean equations, but it becomes difficult to manage when number of variables exceed 5 or 6. So, a technique called Variable Entrant Map (VEM) is used to increase the effective size of k-map. It allows a smaller map to handle large number of variables. This is done by writing output in terms of input.

5 Consider the following logic function. [10] CO2 L3,L2

F(*A*, *B*, *C*, *D*)=*m*(0, 4, 5, 10, 11, 13, 14, 15)
(a) Find two different minimum circuits which implement *F* using AND and OR gates. Identify two hazards in each circuit
(b) Find an AND-OR circuit for *F* which has no hazards.(hazard cover)
(c) Find an OR-AND circuit for *F* which has no hazards. .(hazard cover)

Solution :

(a)

Map

	C'D'	C'D	C.D	C.D'
A'B'	1	0	0	0
A'B	1	1	0	0
A.B	0	1	1	1
AB'	0	0	1	1

Map Layout

	C'D'	C'D	C.D	C.D'

A’B’	0	1	3	2
A’B	4	5	7	6
A.B	12	13	15	14
AB’	8	9	11	10

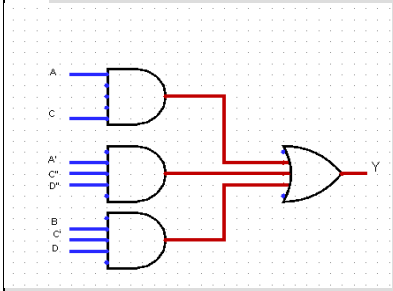
Groups

(10,11,14,15)	A.C	
(0,4)	A’.C’.D’	
(5,13)	B.C’.D	
(4,5)	A’BD	STATIC-1 COVER
(15,13)	ABD	STATIC-1 COVER

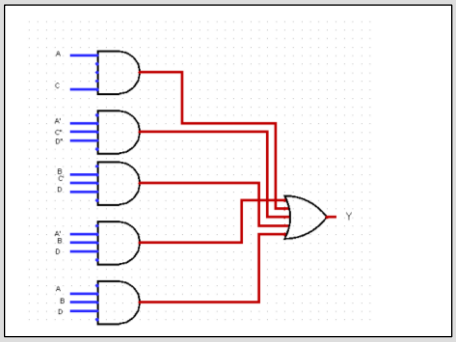
Minimize SOP expression Y = AC + A'C'D' + BC’D

Implement using AND-OR circuit as follows

1.



2.



(b)Recover Static -1 in SOP are = AC + A'C'D' + BC'D+ A’BD+ ABD

2.

(a)PRODUCT of SUMS

Map

	C’D’	C’D	C.D	C.D’
A’B’	1	0	0	0
A’B	1	1	0	0
A.B	0	1	1	1
AB’	0	0	1	1

Map Layout

	C’D’	C’D	C.D	C.D’
A’B’	0	1	3	2
A’B	4	5	7	6
A.B	12	13	15	14
AB’	8	9	11	10

Groups

(2,3,6,7)	A.C

		(1,9)	B’.C’.D			
		(8,12)	A.C’.D’			

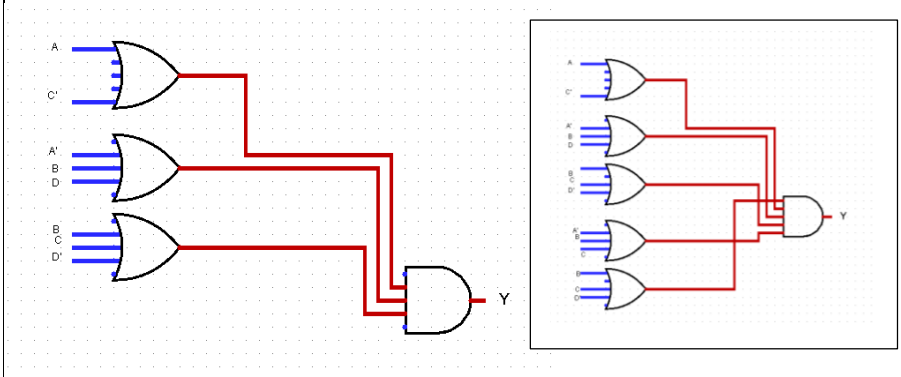
$\underline{y} = A.C + B'.C'.D + A.C'.D'$

$y = \overline{A.C + B'.C'.D + A.C'.D'}$

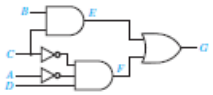
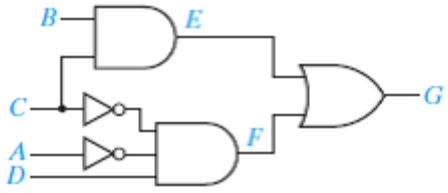
Minimize POS expression Y = (A + C') (B + C + D') (A' + C + D)

Implement using OR-AND circuit as follows

1. **2.**



2.Recover Static -1 in POS are =(A + C') (B + C + D') (A' + C +D)(A’+B+C)(B+C+D’)

6	What is the use of simulation software? For the following circuit (a) Assume that the inverters have a delay of 1 ns and the other gates have a delay of 2 ns. Initially *A* =0 and *B*=*C*=*D* =1, and *C* changes to 0 at time =2 ns. Draw a timing diagram and identify the transient that occurs.  (b) Modify the circuit to eliminate the hazard. **Solution :** Simulation is a decision analysis and support tool. Simulation software allows you to evaluate, compare and optimize alternative designs, plans and policies (a)  	[5+5]	CO2	L1,L2,L3

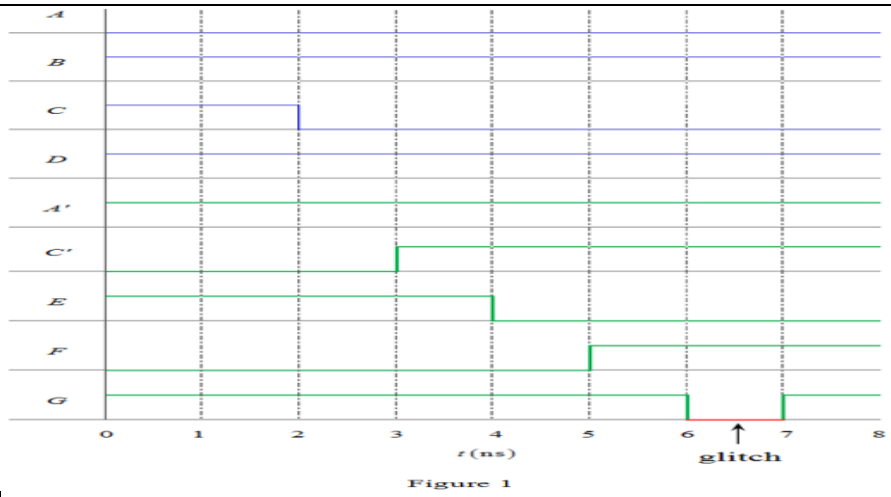


Figure 1

(b) **Recover Hazard circuit as below**