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Internal Assessment Test 1 – December 2022

Sub:	Analog and Digital	Electronics				Sub Code:	21CS33	Branch	: ISE		
Date:	02/12/2022	Duration:	90 min's	Max Marks:	50	Sem/Sec:	III / A,B and (C		0	BE
		Ans	swer any FIV	E FULL Quest	<u>ions</u>				MARKS	CO	RBT
1	With the help of	f flow chart	explain ho	w to determin	e Mi	nimum Sur	n of Products	susing	10	CO3	L3
	a Karnaugh Map	with an Ex	ample.								
2	What are the disa	advantages	of K map?	Find the mini	mun	SOP expre	ession using (QM	10	CO3	L3
	method for the fo	ollowing fu	nction f (a,	$b, c, d) = \sum m$	(0,1,	2,3,10,11,12	2,13,14,15)				
3	Minimize the fo	ollowing fu	nction for S	SOP using K r	nap	and realize	it by using b	asic	10	CO3	L3
	gates f (a,b,c,d)	$= \pi M (5,7)$	7,13,14,15)	+d(1,2,3,9)							
4	Realize basic gates	s and Ex-Or	using NANI	O and NOR gat	es or	ıly.			10	CO4	L3
5	What is Hazard? elimination meth	_	tatic 0 and S	Static 1 hazaro	d wit	h an examp	ole and its		10	CO4	L2
6	Implement the	following	Boolean fi	unction using	8:1	Mux f(a,	b, c, d) = 2	Σm	10	CO3	L3
	(0,1,2,4,6,9,12,14	4)									

CCI Signature

HOD Signature

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Faculty Signature

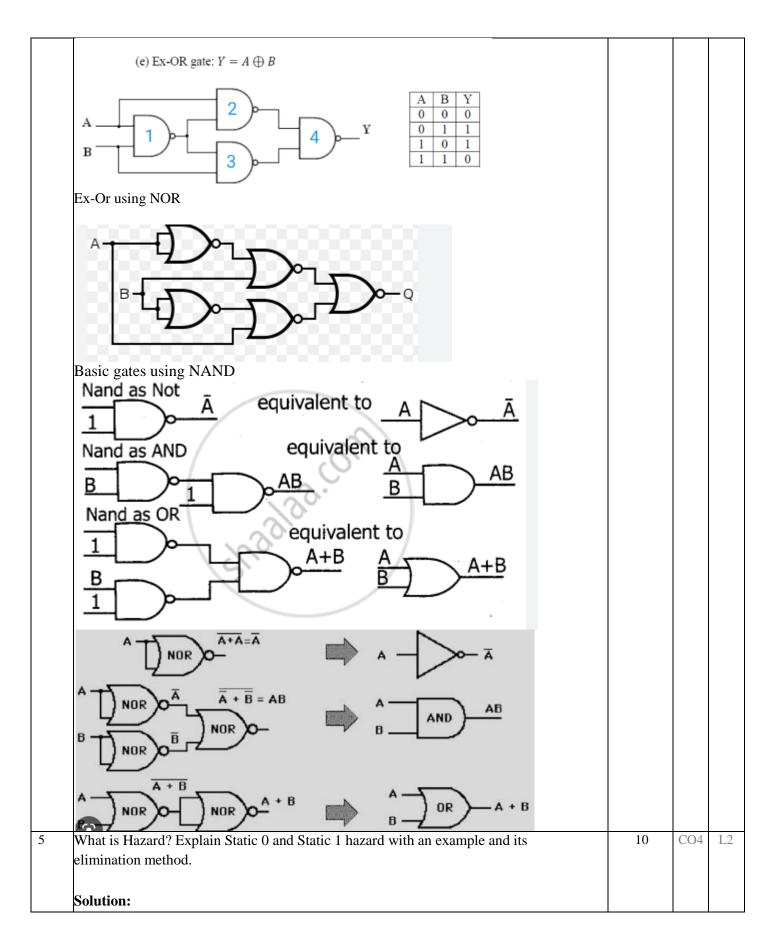
CCI Signature

HOD Signature

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Internal	Assessment Test I –	 -December (2022		ACCREDITED W	TH A+ GRADE B	Y NAAC
Sub: Analog and Digital Electronics	7 ISSESSMENT TEST 1	Sub Code:	21CS33	Branch	: ISE		
Date: 02/12/2022 Duration: 90 min's	Max Marks: 50	Sem/Sec:	III / A, B and C		. ISE	OB	E
	FIVE FULL Questions	Sem see.	111 / 11, B una (IARKS		RB
With the help of flow chart explain he Karnaugh Map with an Example.	ow to determine Mini	mum Sum of	f Products using	ıg a	10	CO3	Ι
Solution:							i
Choose a 1 which has not been covered. Find all adjacent 1's and X's. Are the chosen 1 and its adjacent 1's and X's covered by a single term? YES That term is an essential prime implicant. Loop it. Note: All esse implicants have determined at determined at find a minimum set of prime implicants which cover the remaining 1's on the map.	All prime implicants: A' All prime implicants: A' AB TB TB TB TB TB TB TB TB TB	TO CD CD 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1					
What are the disadvantages of K map method for the following function f (a					10	CO3	L
Solution:	, , , , (-j- j-	, , , , -,-	, , ,				'n
Disadvantages of K map:							i
The Karnaugh map method is an	effective way to	simplify sw	itching funct	ions			ì
which have a small number of var	<u> </u>		•				ı
			_				ì
if several functions must be simpli	neu, me use of a dig	gitai comput	ei is desirable	₹.			ì

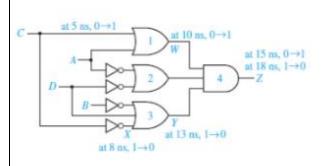
Determination of PI:

	ge 1		tage 2	inan	Stage 3		
<i>ABCD</i> 0 0 0 0	minterms (0)√	<i>ABCD</i> 0 0 0 -	minterms	ABCD 0 0	minterms		
	(0)	00-0	(0,1)√ (0,2)√	00	(0,1,2,3) (0,2,1,3)		
0001	(1)√ (2)√	00-1	(1,3)√ (2,3)√	-01-	(2,10,3,11)		
0 0 1 1 1 0 1 0 1 1 0 0	(3)√ (10)√ (12)√	-010 -011 101-	(2,10)√ (3,11)√ (10,11)√	1-1- 1-1- 11 11	(10,11,14,15) (10,14,11,15) (12,13,14,15) (12,14,13,15)		
1011	(11)√ (13)√	1 - 1 0 1 1 0 - 1 1 - 0	(10,14)√ (12,13)√ (12,14)√				
1111	(14)√ (15)√	1 - 1 1 1 1 - 1 1 1 1 -	(11,15)√ (13,15)√ (14,15)√	====			
Prime implica	ant charts:						
B'C (2,3	11 14 15)		V V	V V			
AC (10, AB (12,1	11,14,15) 13,14,15) B'C + AB o	r Y = A'B' +	N N N AC+AB	1 1 1			
AC (10, AB (12, 13)) $Y = A'B' + A$	$B'C + AB \text{ of following } AB, AB = \pi M \text{ (}$	function for 5,7,13,14,15	Synthesis I I I Co. Antiki	akes the	ize it by using basic	6	CO3
AC (10, AB (12, Y = A'B' + Minimize the gates f (a,b,c. Solution:	B'C + AB of e following e,d) = π M (function for $5,7,13,14,15$ A B OO OI X 11 X F = $\frac{1}{2}$ N) Indicates a corresponding	SOP using K r 5) +d(1,2,3,9). 01 11 10 0 0 X 0 0 1 1 0 1 1 1 0 1 A'D' + B' + C'D' minterm that ma	akes the essential. or m ₁₁		10	

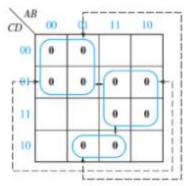


When the input to a combinational circuit changes, unwanted switching transients may appear in the output. These transients occur when different paths from input to output have different propagation delays.

- If, in response to any single input change and for some combination of propagation delays, a
 circuit output may momentarily go to 0 when it should remain a constant 1, we say that the circuit
 has a static 1-hazard.
- Similarly, if the output may momentarily go to 1 when it should remain a 0, we say that the circuit has a static 0-hazard.
- o If, when the output is supposed to change from 0 to 1 (or 1 to 0), the output may change three or more times, we say that the circuit has a dynamic hazard.



(a) Circuit with a static 0-hazard



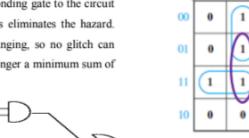
(b) Karnaugh map for circuit of (a)

<u>Detection of Static 1 Hazard:</u> Hazards can be detected using a Karnaugh map (see above Figure). As seen on the map, no loop covers both minterms ABC and ABC'. So if A = C = 1 and B changes, both terms can momentarily go to 0, resulting in a glitch in F.

We can detect hazards in a two-level AND-OR circuit, using the following procedure:

- 1. Write down the sum-of-products expression for the circuit.
- 2. Plot each term on the map and loop it.
- If any two adjacent 1's are not covered by the same loop, a 1-hazard exists for the transition between the two 1's. For an n-variable map, this transition occurs when one variable changes and the other n – I variables are held constant.

To Eliminate Static 1 Hazard: If we add a loop to the map of above Figure and, then, add the corresponding gate to the circuit (as shown in the following Figure), this eliminates the hazard. The term AC remains I while B is changing, so no glitch can appear in the output. Note that F is no longer a minimum sum of products.



Detection of Static 0 Hazard: The following Figure shows a circuit with several 0-hazards. The product-of-sums representation for the circuit output is F = (A + C)(A' + D')(B' + C' + D)

