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Internal Assessment Test 2 – December 2022

Sub:	Analog and Digital Electronics				Sub Code:	18CS33	Branch:	ISE
Date:	27/12/2022	Duration:	90 min’s	Max Marks:	50	Sem/Sec:	III / A,B and C	OBE

	Answer any FIVE FULL Questions	MARKS	CO	RBT
1	Explain the structure of VHDL Program. Write VHDL Code for 4-bit full subtractor.	10	CO5	L2
2	Design 7 segment decoder and realize using PLA	10	CO4	L3
3	Construct and explain SR gate latches using NAND gates and derive the characteristics equation for the same	10	CO4	L2
4	Differentiate between PAL and PLA. Realize the following functions using PLA. F(a, b, c, d) = m(1,2,4,5,6, 8,10,12,14) and F(a, b, c, d) = m(1,2,4,6,8,10,11,12,14,15)	10	CO4	L2
5	Design full subtractor circuit using decoder and NAND gates	10	CO4	L3
6	Design 8:1 MUX, using conditional signal assignment statement and selected signal assignment statement.	10	CO4	L3

Faculty Signature CCI Signature HOD Signature

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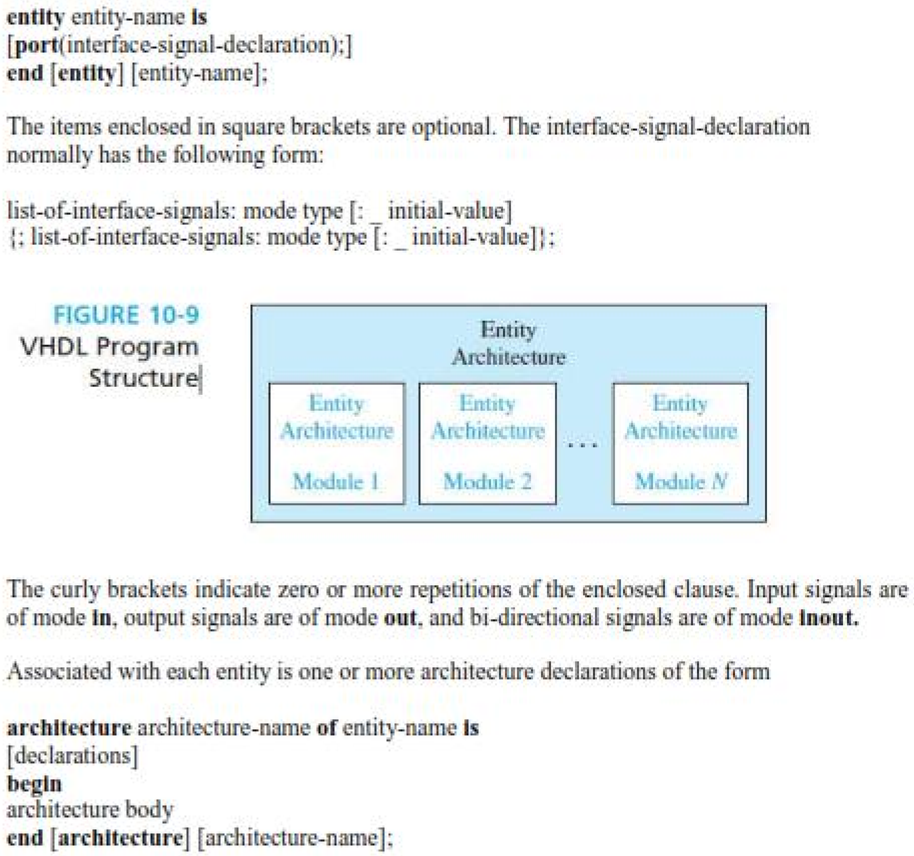
Internal Assessment Test II –December 2022

Sub:	Analog and Digital Electronics					Sub Code:	21CS33	Branch: ISE
Date:	27/12/2022	Duration:	90 min's	Max Marks:	50	Sem/Sec:	III / A, B and C	OBE

	Answer any FIVE FULL Questions	MARKS	CO	RBT
1	Explain the structure of VHDL Program. Write VHDL Code for 4-bit full subtractor.	10	CO5	L2

Solution:



entity entity-name **is**
[**port**(interface-signal-declaration);]
end [**entity**] [entity-name];

The items enclosed in square brackets are optional. The interface-signal-declaration normally has the following form:

list-of-interface-signals: mode type [: _ initial-value]
{; list-of-interface-signals: mode type [: _ initial-value]};

FIGURE 10-9 VHDL Program Structure

Entity
Architecture
Entity
Architecture
Module 1
Entity
Architecture
Module 2
. . .
Entity
Architecture
Module N

The curly brackets indicate zero or more repetitions of the enclosed clause. Input signals are of mode **in**, output signals are of mode **out**, and bi-directional signals are of mode **inout.**

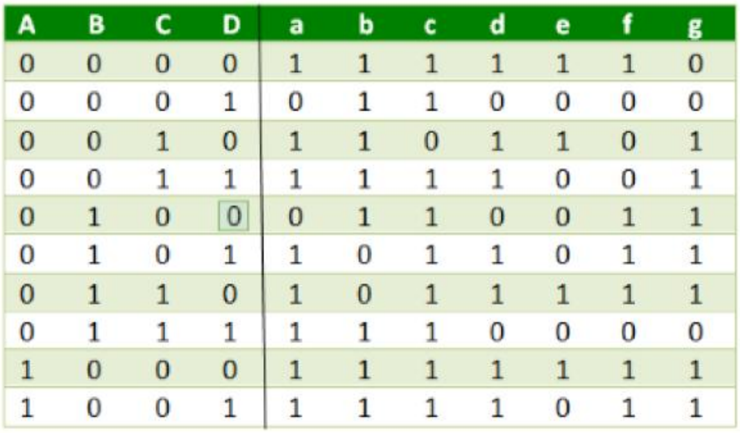
Associated with each entity is one or more architecture declarations of the form

architecture architecture-name **of** entity-name **is**
[declarations]
begin
architecture body
end [**architecture**] [architecture-name];

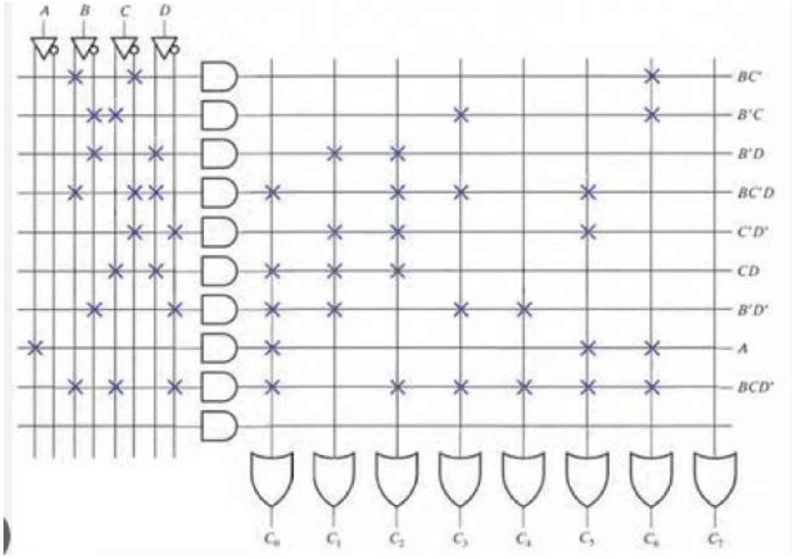
```
entity half_sub is

port ( a,b : in std_logic;

           dif,bo: out std_logic );

end half_sub;

architecture sub_arch of half_sub is

  begin

     dif <= a xor b;

     bo <= (not a) and b;

end sub_arch;
```

2	Design 7 segment decoder and realize using PLA	10	CO4	L3

Solution:



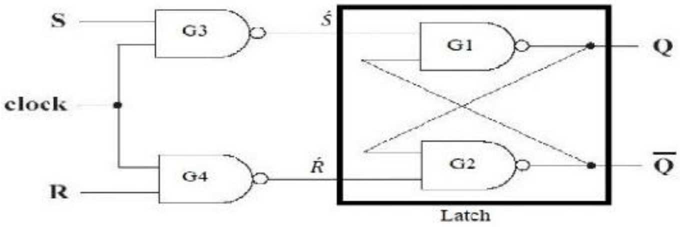
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

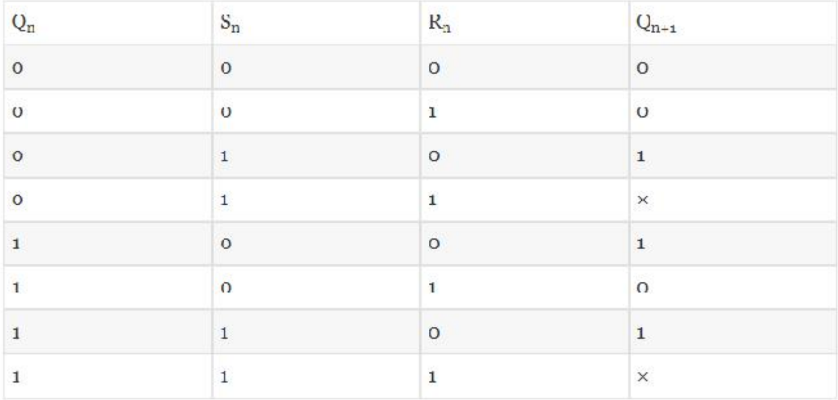


3	Construct and explain SR gate latches using NAND gates and derive the characteristics equation for the same.	6	CO4	L2

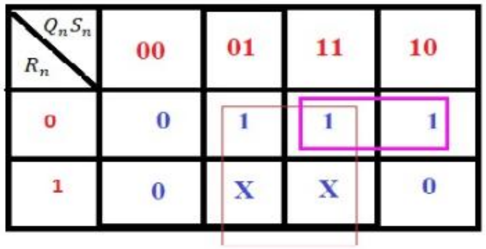
Solution:

In the SR flip flop we will use the SR latch using NAND gate and two extra NAND gate will be used which are G3 and G4. The input to G3 and G4 will be S and R respectively and clock signal is applied to both gates which will be train of pulses.

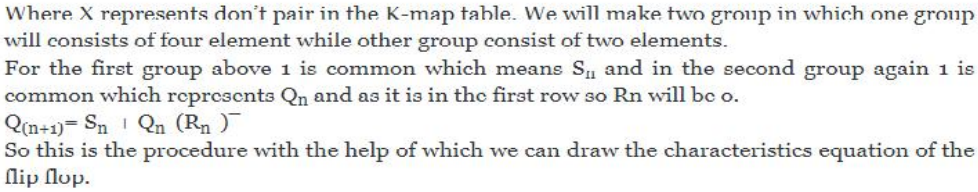




Q_n	S_n	R_n	Q_{n-1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	×
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	×



Q_nS_n / R_n	00	01	11	10
0	0	1	1	1
1	0	X	X	0



Where X represents don't pair in the K-map table. We will make two group in which one group will consists of four element while other group consist of two elements.

For the first group above 1 is common which means S_n and in the second group again 1 is common which represents Q_n and as it is in the first row so Rn will be 0.

$Q_{(n+1)}= S_n + Q_n\ (R_n\ )^{-}$

So this is the procedure with the help of which we can draw the characteristics equation of the flip flop.

4	Differentiate between PAL and PLA. Realize the following functions using PLA. F(a, b, c, d) = m(1,2,4,5,6, 8,10,12,14) and F(a, b, c, d) = m(1,2,4,6,8,10,11,12,14,15)	10	CO4	L2

Solution:

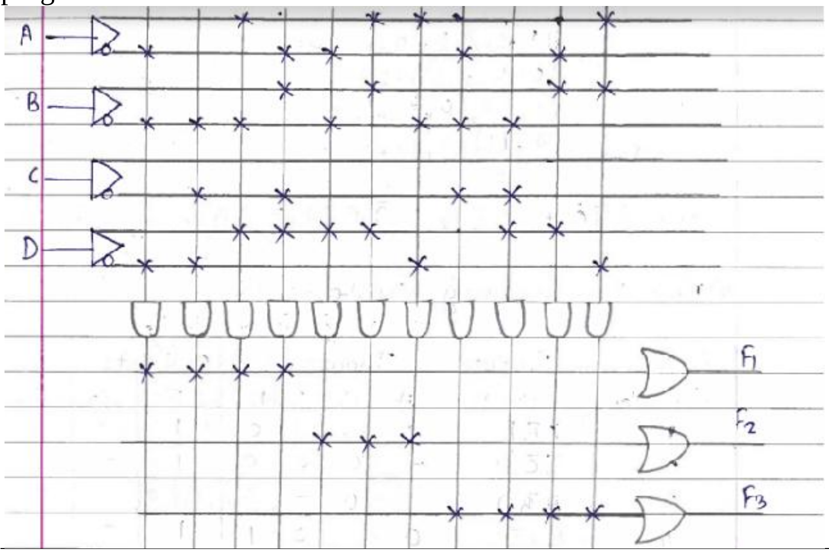
Programmable Logic Arrays (PLA):

A *PLA* with *n* inputs and *m* outputs can realize *m* functions of *n* variables. In PLA, the product terms of the input variables is realized by an AND array; and the OR array ORs together the product terms needed to form the output functions. Hence, a PLA implements a sum-of-products expression.

Programmable Array Logic (PAL):

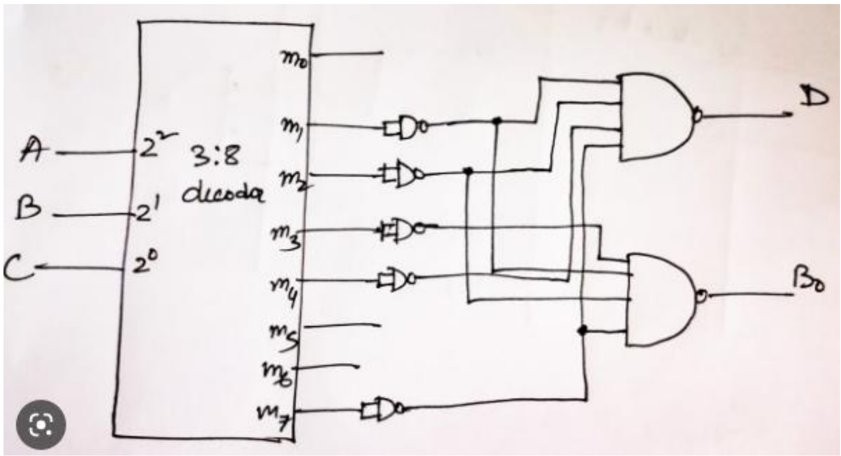
A *PAL* is a special case of the programmable logic array (PLA) in which the AND array is programmable

and the OR array is fixed. The following Figure represents a segment of an un-programmed PAL.



5	Design full subtractor circuit using decoder and NAND gates.	10	CO4	L3

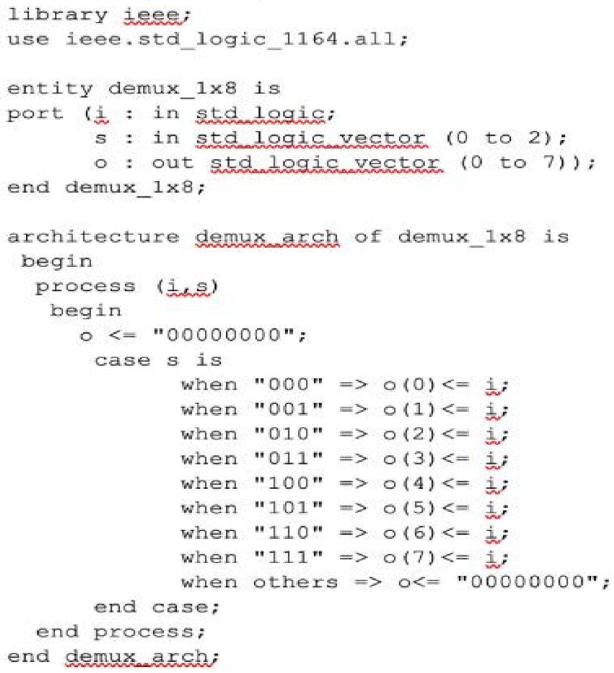
Solution:



6	Design 8:1 MUX, using conditional signal assignment statement and selected signal assignment statement.	10	CO4	L3

Solution:

conditional signal assignment statement



```
library ieee;
use ieee.std_logic_1164.all;

entity demux_1x8 is
port (i : in std_logic;
      s : in std_logic_vector (0 to 2);
      o : out std_logic_vector (0 to 7));
end demux_1x8;

architecture demux_arch of demux_1x8 is
 begin
  process (i,s)
   begin
     o <= "00000000";
      case s is
            when "000" => o(0)<= i;
            when "001" => o(1)<= i;
            when "010" => o(2)<= i;
            when "011" => o(3)<= i;
            when "100" => o(4)<= i;
            when "101" => o(5)<= i;
            when "110" => o(6)<= i;
            when "111" => o(7)<= i;
            when others => o<= "00000000";
      end case;
  end process;
end demux_arch;
```

selected signal assignment statement.

```
Entity mux ;
    Port (S0: in STD_LOGIC;
    S1 :in STD_LOGIC;
    S2 :in STD_LOGIC;
 IN0 :in STD_LOGIC;
   IN1 :in STD_LOGIC;
   IN2 :in STD_LOGIC;
   IN3 :in STD_LOGIC;
   IN4 :in STD_LOGIC;
 IN5 :in STD_LOGIC;
 IN6 :in STD_LOGIC;
 IN7 :in STD_LOGIC;
 Y :out STD_LOGIC );
End mux ;


Architecture behavioral of mux is
   Signal a0,a1,a2,a3,a4,a5,a6,a7:BIT;
  begin
  a0 <= IN0  and (not s0)  and  (not s1)  and  (not s2);
  a1 <= IN1  and (not s0)  and  (not s1)  and        s2;
  a2 <= IN2  and (not s0)  and        s1    and  (not s2);
  a3 <= IN3  and (not s0)  and        s1    and        s2;
  a4 <= IN4  and      s0      and  (not s1)  and  (not s2);
  a5 <= IN5  and      s0      and  (not s1)  and        s2;
  a6 <= IN6  and      s0      and         s1   and  (not s2);
  a7 <= IN7  and      s0      and         s1   and        s2;

  Y <= a0 or a1 or a2 or a3 or a4 or a5 or a6 or a7
  end behavioral;
```