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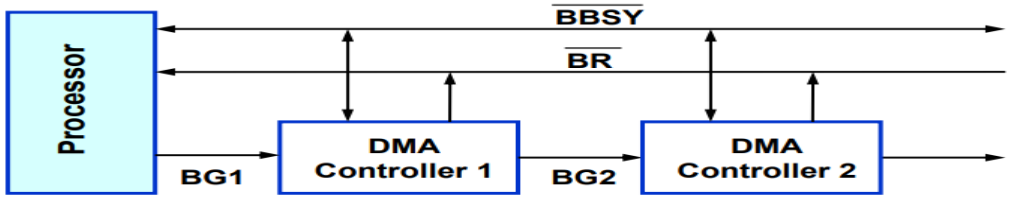
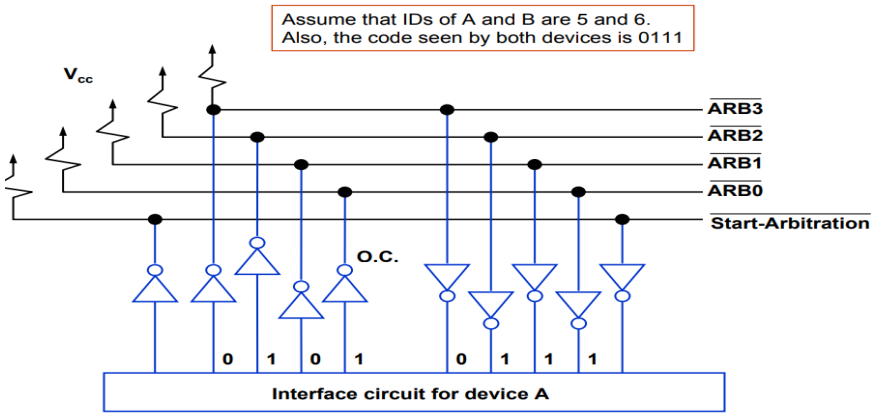
Internal Assessment Test 2 – December 2022

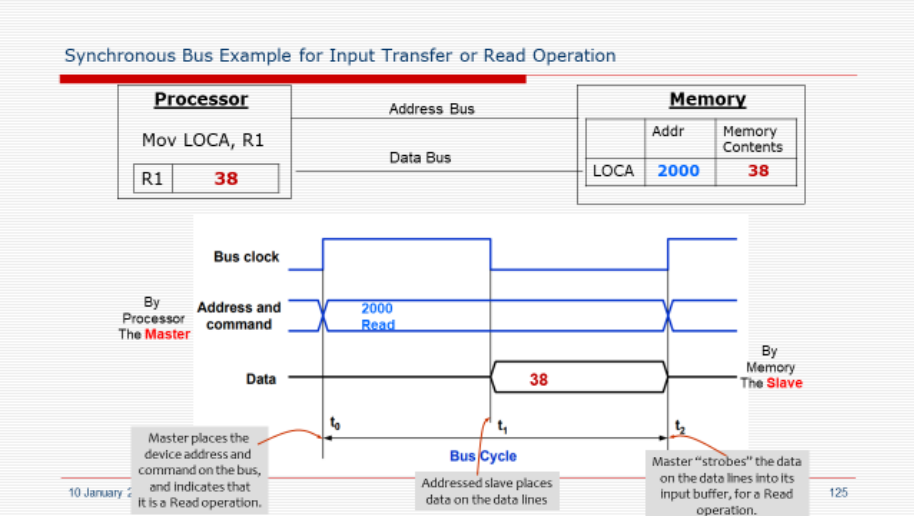
Scheme and Solution

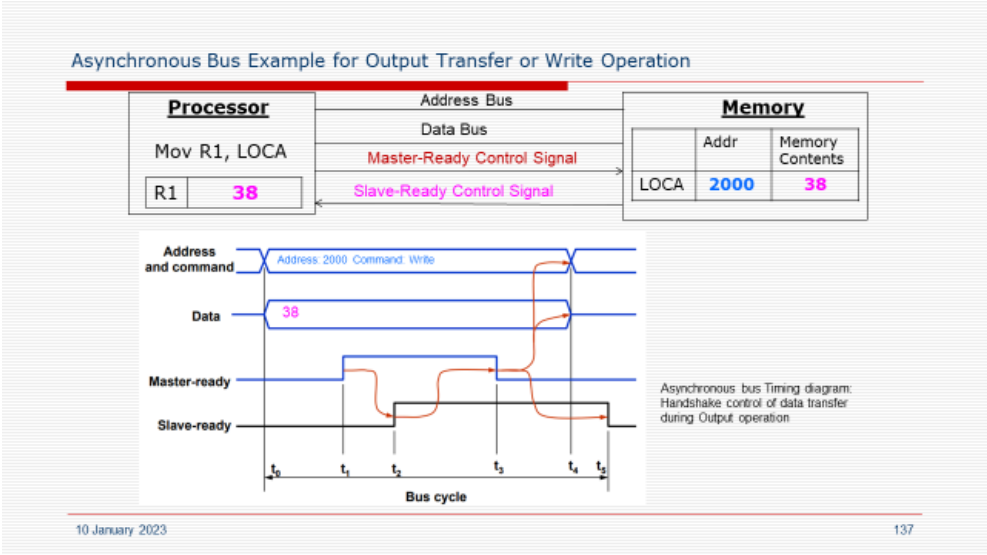
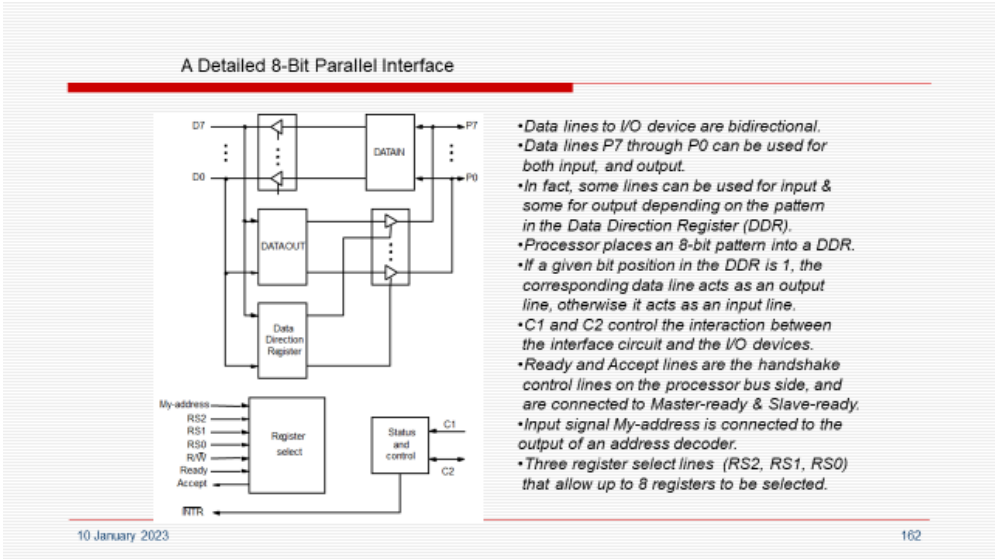
Sub:	Computer Organization and Architecture					Sub Code:	21CS34	Branch:	CSE	
Date:	27/12/22	Duration:	90 minutes	Max Marks:	50	Sem / Sec:	III / A, B, C		OBE	

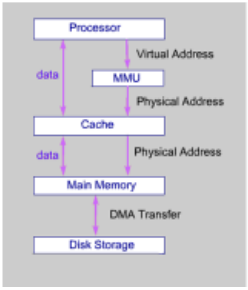
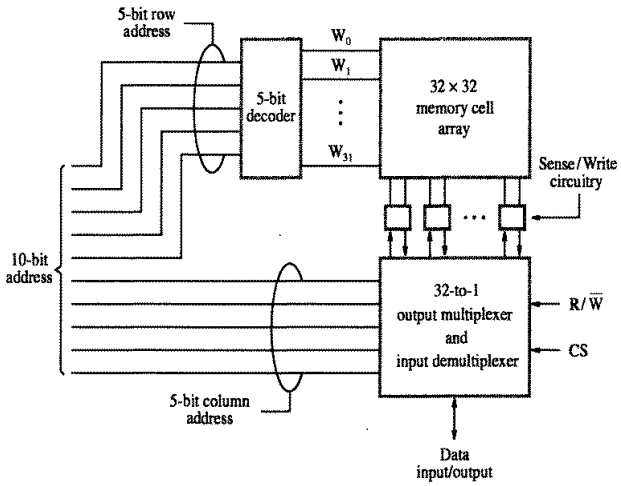
	Answer any FIVE FULL Questions	MARKS	CO	RBT
1	What is the process needed to resolve the conflict when more than one device try to use the bus to access main memory? Explain any 2 approaches in detail with figure. **Bus Arbitration – 2 Marks** The process by which the next device to become the bus master is selected and bus mastership is transferred to it is called bus arbitration. Two approaches for Bus arbitration **1. Centralized arbitration: 4 Marks** A single bus arbiter performs the arbitration. Usually Processor will be the Bus arbiter  • A single bus-arbiter performs the required arbitration • Normally, processor is the bus-master. • Processor may grant bus-mastership to one of the DMA controllers. • A DMA controller indicates that it needs to become bus-master by activating BR line. • The signal on the BR line is the logical OR of bus-requests from all devices connected to it. • Then, processor activates BG1 signal indicating to DMA controllers to use bus when it becomes free. • BG1 signal is connected to all DMA controllers using a daisy-chain arrangement. • If DMA controller-1 is requesting the bus, Then, DMA controller-1 blocks propagation of grant-signal to other devices. Otherwise, DMA controller-1 passes the grant downstream by asserting BG2. • Current bus-master indicates to all devices that it is using bus by activating BBSY line. • The bus-arbiter is used to coordinate the activities of all devices requesting memory transfers. • Arbiter ensures that only 1 request is granted at any given time according to a priority scheme. (BR → Bus-Request, BG → Bus-Grant, BBSY → Bus Busy). **2. Distributed arbitration: 4 Marks** All devices participate in the selection of the next bus master.	[10]	2	L2



- Assume that two devices, A and B, having ID numbers 5 and 6, respectively, are requesting the use of the bus.
- Device A transmits the pattern 0101, and device B transmits the pattern 0110.
- The code seen by both devices is 0111. (Logical OR of the IDs of 2 devices)
- Each device compares the pattern on the arbitration lines to its own ID, starting from the most significant bit.
- If it detects a difference at any bit position, it disables its drivers at that bit position and for all lower-order bits. It does so by placing a 0 at the input of these drivers.
- In the case of our example, device A detects a difference on line ARB 1. Hence, it disables its drivers on lines ARB1 and ARB0.
- This causes the pattern on the arbitration lines to change to 0110, which means that B has won the contention.

2	(a) Mov LOCA, R1 With the help of timing diagram, Show how the input transfer or read operation in the given instruction will happen if all the devices derive timing information from a common clock line. **Synchronous Data Transfer – Diagram and Explanation – 5 Marks** 	[5]	2	L2

	• The picture shows two views of the signal except the clock • One view shows the signal seen by the master & the other is seen by the salve. • Master sends the address & command signals on the rising edge at the beginning of clock pe • These signals do not actually appear on the bus until t_{am}. • Sometimes later, at t_{AS} the signals reach the slave. • The slave decodes the address. • At t_1, the slave sends the requested-data. • At t_2, the master loads the data into its input-buffer. • Hence the period t_2, t_{DM} is the setup time for the master's input-buffer. • The data must be continued to be valid after t_2, for a period equal to the hold time of that bu **Disadvantages** • The device does not respond. • The error will not be detected.			
	(b) Mov R1, LOCA With the help of timing diagram, Show how the output transfer or write operation in the given instruction will happen if there is no clock signal between the sender and receiver. **Asynchronous Data Transfer – Diagram and Explanation – 5 Marks** 	[5]	2	L2
3	(a) With neat diagram, explain the general 8 bit parallel interface circuit. **Diagram and Explanation – 5 Marks** 	[5]	2	L1

	(b) What is Virtual Memory? Explain its basic organization with neat diagram. **Diagram and Explanation – 5 Marks** **VIRTUAL MEMORY** • Virtual memory – separation of user logical memory from physical memory. • Only part of the program needs to be in memory for execution. • Logical address space can therefore be much larger than physical address space. • Allows address spaces to be shared by several processes. • Allows for more efficient process creation. • A special hardware unit, called the **Memory Management Unit (MMU),** translates virtual addresses into physical addresses.  	[5]	3	L1
4	(a) Explain the organization of 1K x 1 memory chip **Diagram and Explanation – 5 Marks**  **Figure 5.3** Organization of a 1K × 1 memory chip.	[5]	3	L1
	(b) With a neat diagram briefly explain the internal organization of 16 Megabit dynamic memory chip configured as 2M x 8 **Diagram and Explanation – 5 Marks**	[5]	3	L1

ASYNCHRONOUS DRAMS

- The 4 bit cells in each row are divided into 512 groups of 8 (Figure 5.7).
- 21 bit address is needed to access a byte in the memory. 21 bit is divided as follows
  1) 12 address bits are needed to select a row.
     i.e. A_{8-0} → specifies row-address of a byte.
  2) 9 bits are needed to specify a group of 8 bits in the selected row.
     i.e. A_{20-9} → specifies column-address of a byte.

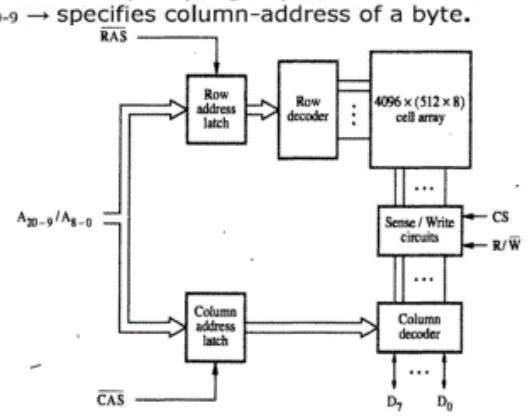


Figure 5.7 Internal organization of a 2M x 8 dynamic memory chip.

(a) With a neat diagram explain the internal structure of Synchronous DRAM.
Diagram and Explanation – 5 Marks

SYNCHRONOUS DRAMS

- The operations are directly synchronized with clock signal (Figure 8.8).
- The address and data connections are buffered by means of registers.
- The output of each sense amplifier is connected to a latch.
- A Read-operation causes the contents of all cells in the selected row to be loaded in these latche
- Data held in latches that correspond to selected columns are transferred into data-output regist
- Thus, data becoming available on the data-output pins.

- First, the row-address is latched under control of RAS" signal (Figure 8.9).
- The memory typically takes 2 or 3 clock cycles to activate the selected row.
- Then, the column-address is latched under the control of CAS" signal.
- After a delay of one clock cycle, the first set of data bits is placed on the data-lines.
- SDRAM automatically increments column-address to access next 3 sets of bits in the selected row.

5 [5] 3 L1

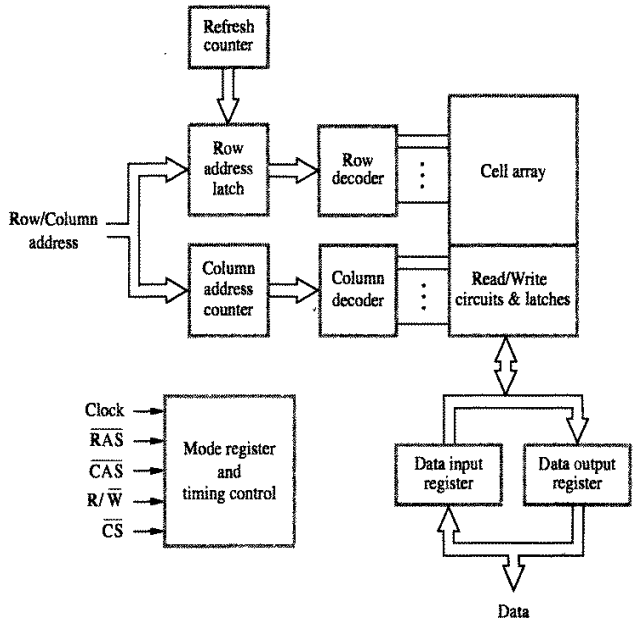
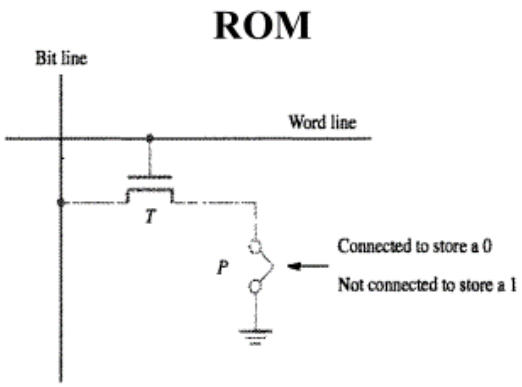


Figure 5.8 Synchronous DRAM.

	(b) Analyze how data are written into Read Only Memories. Discuss the different types of Read Only Memories.
	
	ROM Cell – 2 Marks
	
	 
	
	Figure 5.12 A ROM cell.
	
	➢ **At Logic value '0'** → Transistor(T) is connected to the ground point (P). Transistor switch is closed & voltage on bit-line nearly drops to zero
	➢ **At Logic value '1'** → Transistor switch is open. The bit-line remains at high voltage.
	
	Types of ROM with explanation – 3 Marks
	
	• ROM
	  • PROM (Programmable Read Only Memory)
	  • EPROM (Erasable Programmable Read Only Memory)
	  • EEPROM (Electrically Erasable Programmable Read Only Memory)
	  • Flash
	  • Flash Cards
	  • Flash Drives
		[5]	3	L2

6	(a) Consider the following 2 scenarios and answer the questions under each. A cache is organized in direct-mapped manner with the following parameters: Main memory size 32K words; Cache size 512 words; Block size 64 words (i) How many bits are there in a main memory address? (ii) How many bits are there in each of the TAG, BLOCK and WORD fields? **MAIN MEMORY** Total Size – 32,768 That can be represented with 2^x addresses Therefore Address length = **15 bits**. (2^{15} = 32,768) **WORD** 64 Words per block 6 **bits** for WORD field (2^6 = 64) **BLOCK** No. of Blocks = Total Cache Size / Words per block = 1024 / 128 = **8** **3 bits** for BLOCK field (8 Blocks = 2^3 = 8) **TAG** Remaining **6 bits** for TAG field.	[5]	3	L3

	A block-set-associate cache consists of a total of 128 blocks divided into 8-block sets. The main memory contains 4096 blocks, each consisting of 128 words. (i) How many bits are there in a main memory address? (ii) How many bits are there in each of the TAG, SET and WORD fields? **Answer** Main Memory size=4096 blocks x128 words =4 x 1024 x 128 $=2^2 \times 2^{10} \times 2^7 = 2^{19}$ Hence number of bits for address is **19-bits** Word – 7 Set – 4 Tag – 8 bit			
	(b) Define the following with respect to cache memory (i) Mapping Function (ii) Replacement Algorithm (iii) Stale Data (iv) Write Through Protocol (v) Write Back Protocol **Each 1 Mark** (i) Mapping Function At any given time, only some blocks in the main memory are held in the cache. Which blocks in the main memory are in the cache is determined by a "**mapping function**". (ii) Replacement Algorithm When the cache is full, and a block of words needs to be transferred from the main memory, some block of words in the cache must be replaced. This is determined by a "**replacement algorithm**". (iii) Stale Data During a DMA transfer from Main Memory to Disk and the cache uses write-back protocol, the data in memory might not reflect the changes that have been made in the cached copy. That outdated data in the memory is called the stale data (iv) Write Through Protocol Contents of the cache and the main memory may be updated simultaneously. This is the write-through protocol. (v) Write Back Protocol Update the contents of the cache, and mark it as updated by setting a bit known as the **dirty bit** or **modified bit**. The contents of the main memory are updated when this block is replaced. This is **write-back** or **copy-back protocol**.	[5]	3	L1

CO PO Mapping

Course Outcomes		Modules covered	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
CO1	Explain the organization and architecture of computer systems with machine instructions and programs	**1**	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	Analyze the input/output devices communicating with computer system	**2**	3	-	-	-	-	-	-	-	-	-	-	-	2	-	-	-
CO3	Demonstrate the functions of different types of memory devices	**3**	2	2	2	-	-	-	-	-	-	-	-	-	-	2	-	-
CO4	Apply different data types on simple arithmetic and logical unit	**4**	3	-	-	-	-	-	-	-	-	-	-	-	-	2	-	-
CO5	Analyze the functions of basic processing unit, Parallel processing and pipelining	**5**	3	2	3	2	-	-	-	-	-	-	-	-	-	2	-	-

COGNITIVE LEVEL	REVISED BLOOMS TAXONOMY KEYWORDS
L1	List, define, tell, describe, identify, show, label, collect, examine, tabulate, quote, name, who, when, where, etc.
L2	summarize, describe, interpret, contrast, predict, associate, distinguish, estimate, differentiate, discuss, extend
L3	Apply, demonstrate, calculate, complete, illustrate, show, solve, examine, modify, relate, change, classify, experiment, discover.
L4	Analyze, separate, order, explain, connect, classify, arrange, divide, compare, select, explain, infer.
L5	Assess, decide, rank, grade, test, measure, recommend, convince, select, judge, explain, discriminate, support, conclude, compare, summarize.

PROGRAM OUTCOMES (PO), PROGRAM SPECIFIC OUTCOMES (PSO)				CORRELATION LEVELS	
PO1	Engineering knowledge	PO7	Environment and sustainability	0	No Correlation
PO2	Problem analysis	PO8	Ethics	1	Slight/Low
PO3	Design/development of solutions	PO9	Individual and team work	2	Moderate/ Medium
PO4	Conduct investigations of complex problems	PO10	Communication	3	Substantial/ High
PO5	Modern tool usage	PO11	Project management and finance		
PO6	The Engineer and society	PO12	Life-long learning		
PSO1	Develop applications using different stacks of web and programming technologies				
PSO2	Design and develop secure, parallel, distributed, networked, and digital systems				
PSO3	Apply software engineering methods to design, develop, test and manage software systems.				
PSO4	Develop intelligent applications for business and industry				