CBCS SCHEME

17EE34

USN

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***1. Answer any FIVE full questions, choosing ONE full question from each module.***
2. Missing data, if any, may be suitably assumed.

Module-1

1 a. With a neat diagram, explain emitter stabilized bias circuit. **(07 Marks)**

b. Explain double ended clipper with circuit diagram and waveforms. **(07 Marks)**

c. Design a suitable circuit represented by the box shown in Fig.Q1(c) which has the input and output waveforms as indicated.

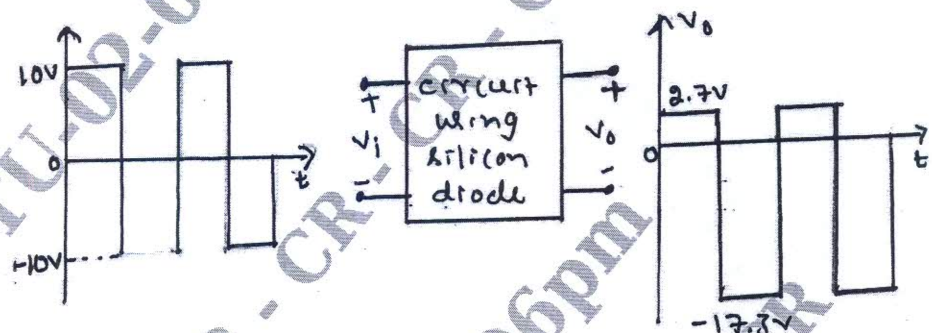

Fig.Q1(c) **(06 Marks)**

OR

2 a. Obtain the expression for stability factors of fixed bias circuit with respect to I_{CO}, V_{BE}, B and draw the circuit diagram. **(08 Marks)**

b. Explain the operation of transistor as switch. **(05 Marks)**

c. For the circuit shown in Fig.Q2(c) using silicon transistor.

i) Find the I_{BQ}, I_{CQ} and V_{CEQ} with $V_{BE} = 0.7$ and $B = 80$

ii) Determine the values of collector, emitter and base voltages with respect to ground.

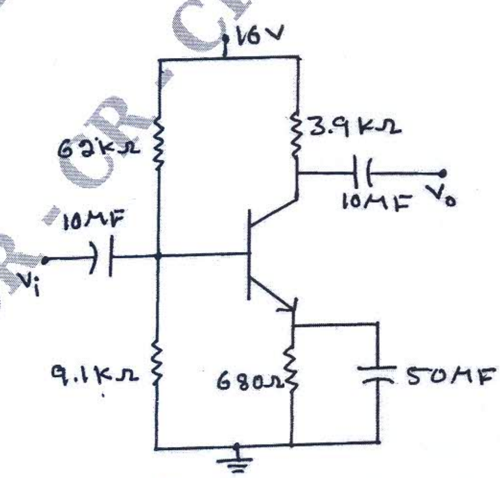

Fig.Q2(c) **(07 Marks)**

Module-2

3 a. Prove that Miller effect of input capacitance is $C_{M_i} = (1 - A_v)_{C_f}$ and output capacitance of $C_{M_0} = \left(1 - \frac{1}{A_V}\right) C_f$. **(06 Marks)**

b. With a neat circuit diagram, derive an expression for Z_i, Z_0, and A_V of fixed bias circuit using hybrid model. **(08 Marks)**

c. For the circuit shown in Fig.Q3(c) calculate : i) Z_i and Z_0 ii) A_v.

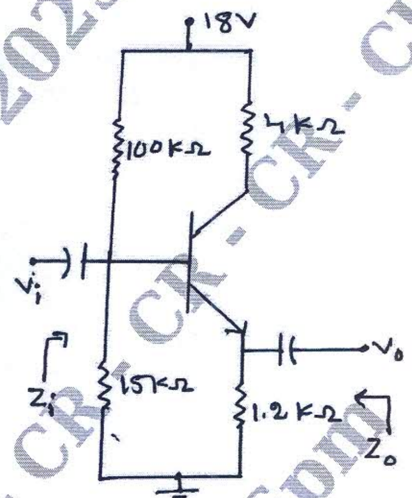

Fig.Q3(c) **(06 Marks)**

OR

4 a. Develop hybrid equivalent circuit of a transistor. Hence draw hybrid models for CB, CE and CC configuration. **(10 Marks)**

b. What are the advantages of h-parameters? **(05 Marks)**

c. Write expressions for :
i) CB parameters interms of CE hybrid parameters
ii) CC parameters interms of CE hybrid parameters. **(05 Marks)**

Module-3

5 a. Draw the circuit of darlington emitter follower. Derive the expression for Z_i, A_I and A_V using its AC equivalent circuit. **(10 Marks)**

b. Derive an expression for input impedance for the voltage series feedback amplifier. **(05 Marks)**

c. Explain the concept of feedback amplifier with simple block diagram. **(05 Marks)**

OR

6 a. Explain the need of cascading amplifier. Draw and explain the block diagram of two stage cascade amplifier. **(06 Marks)**

b. Explain the general characteristics of negative feedback amplifier. **(08 Marks)**

c. Determine the voltage gain, input and output impedance for voltage series feedback having $A = -100$, $R_i = 10K\Omega$ and $R_0 = 20K\Omega$ for feedback. i) $\beta = -0.1$ ii) $\beta = -0.5$. **(06 Marks)**

Module-4

7 a. With neat diagram, explain transformer coupled class A power amplifier and derive the equation for maximum AC output power. **(10 Marks)**

b. Explain the classification of power amplifier with waveforms. **(10 Marks)**

OR

8 a. With neat figure, explain RC phase shift oscillator and derive the expression for frequency of oscillations. **(10 Marks)**

b. A crystal has the following parameters L = 0.334H, C = 0.065PF, C_M = 1PF, R = 5.5KΩ.

i) Calculate the series resonate frequency

ii) Calculate the parallel resonant frequency

iii) By what percent does the parallel resonant frequency exceed the series resonant frequency?

iv) Find the quality factor (Q) of the crystal. **(10 Marks)**

Module-5

9 a. Derive the expression for Z_i, Z_0 and A_v for JFET common source amplifier using fixed bias configuration. **(10 Marks)**

b. For the JFET amplifier shown in Fig.Q9(b).

i) Calculate Z_i and Z_0

ii) Calculate A_V

iii) Calculate Z_i, Z_0 and A_v neglecting the effect of r_d and compare the results.

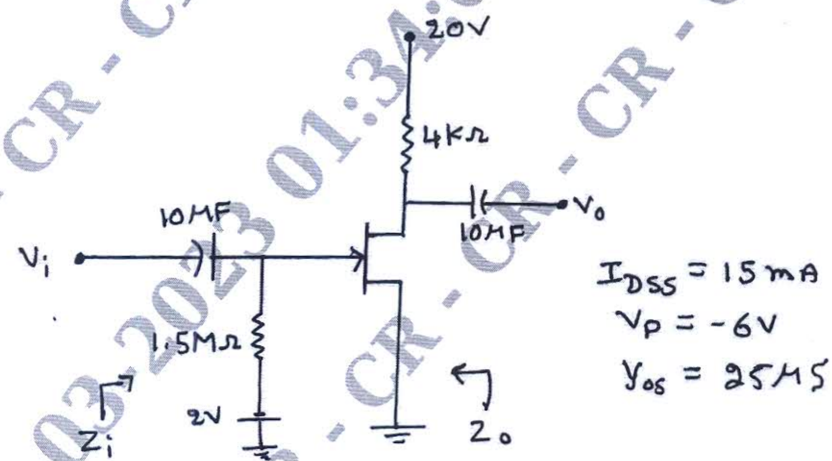

Fig.Q9(b) **(10 Marks)**

OR

10 a. Explain construction and working of MOSFET with characteristics. **(10 Marks)**

b. Explain small-signal model of JFET. **(05 Marks)**

c. Compare JFET and MOSFET. **(05 Marks)**

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