CBCS SCHEME

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17EE35

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Reduce the following function using K-Map technique:
$f(A, B, C, D, E) = \sum m(1, 4, 8, 10, 11, 20, 22, 24, 25, 26) + \sum d(0, 12, 16, 17)$. **(08 Marks)**

b. Design a combinational circuit which takes two, 2 bit binary numbers as its input and generates an output equal to 1, when the sum of the two numbers is odd. **(06 Marks)**

c. With basic block diagram, explain the combinational logic circuit. Differentiate between CLC (Combinational Logic Circuits) and SLC (Sequential Logic Circuits). **(06 Marks)**

OR

2 a. Simplify the following using Quine Mc Cluskey method:
$f(A, B, C, D) = \sum m(1, 2, 3, 5, 9, 12, 14, 15) + \sum d(4, 8, 11)$. **(08 Marks)**

b. Convert the following to its standard canonical form
$f(a, b, c, d) = (a + b + \bar{c})(\bar{b} + \bar{d})(\bar{a} + c)(b + c)$ **(06 Marks)**

c. Reduce the following function using K map technique and implement using basic logic gates: $f(A, B, C, D) = \pi m(0, 2, 4, 10, 11, 14, 15)$. **(06 Marks)**

Module-2

3 a. Implement a full subtractor using an active high output 3:8 decoder. **(07 Marks)**

b. Write the condensed truth table for a 4 to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position or input with highest index and obtain the minimal sum expressions for the outputs. **(07 Marks)**

c. With aid of a block diagram, clearly distinguish between a decoder and an encoder. **(06 Marks)**

OR

4 a. Implement $f(a, b, c, d) = \sum m(0, 5, 7, 8, 9, 12, 15)$ using
i) 8:1 MUX with b, c, d as select lines.
ii) 4:1 MUX with a, d as select lines **(08 Marks)**

b. Design a 1 bit magnitude comparator. **(06 Marks)**

c. Write a short note on look ahead carry adder. **(06 Marks)**

Module-3

5 a. Draw the Master and slave outputs Q and Q′ shown in Fig.Q.5(a). **(06 Marks)**

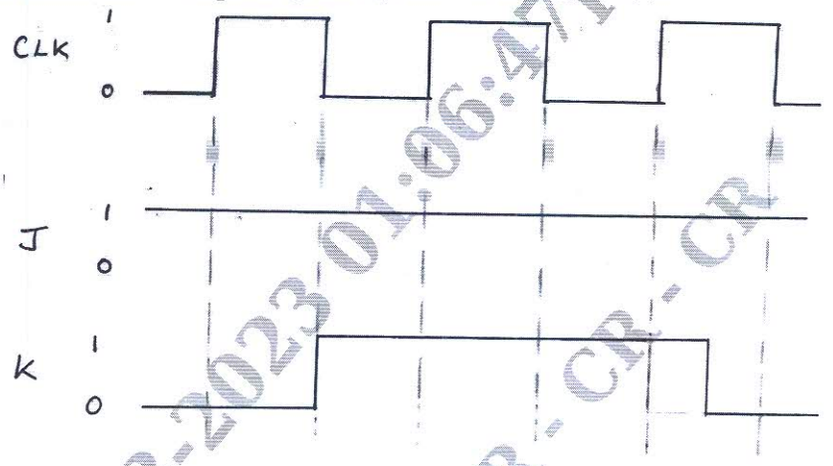

Fig.Q.5(a)

b. Explain the switch debouncer using SR latch and otherwise with waveforms associated with switch debounser. **(06 Marks)**

c. Design a 4 bit shift register using positive edge triggered D flip flops to operate as indicated in the table below:

Table 5(c)

Mode Select		Register operation
S_1	S_0	
0	0	Circular shift left
0	1	Clear
1	0	Complement
1	1	Circular shift right

(08 Marks)

OR

6 a. Design a synchronous Mod-6 counter using SR flip-flops. **(08 Marks)**

b. Draw and explain twisted ring counter in detail. **(06 Marks)**

c. Differentiate between Asynchronous and Synchronous counter. **(06 Marks)**

Module-4

7 a. Explain Mealy model and Moore model in detail. **(08 Marks)**

b. Draw state diagram for circuit shown in Fig.Q.7(b). **(12 Marks)**

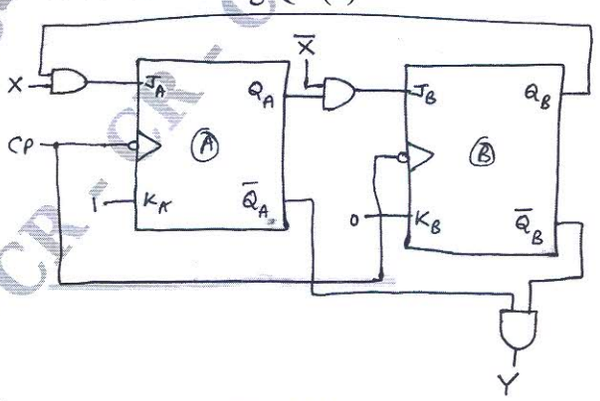

Fig.Q.7(b)

OR

8 a. Design a counter with the sequence 12, 10, 6, 5, 8, 2, 4, 13, 11, 12,….. using T flip-flops. **(10 Marks)**

b. Implement a sequential circuit for state diagram shown in Fig.Q.8(b) using D flip-flops. **(10 Marks)**

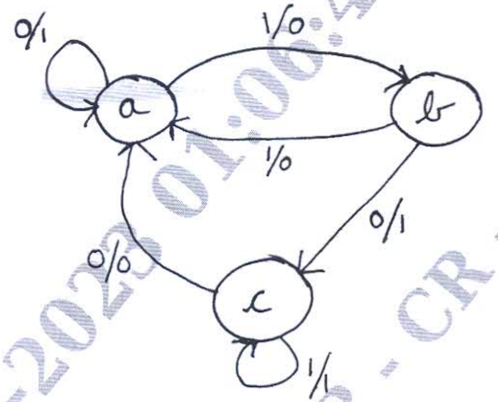

Fig.Q.8(b)

Module-5

9 a. Discuss different operators used in VHDL. **(10 Marks)**

b. Explain the VHDL scalar data types of detail. **(10 Marks)**

OR

10 a. Write a dataflow description (in both VHDL and verilog) for a full adder with active high enable. Draw the truth table and derive the Boolean expression, and verify the circuit. **(10 Marks)**

b. Implement a 4 × 1 multiplexer using VHDL code and also verilog. **(10 Marks)**

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