CBCS SCHEME

USN

18EE34

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the operation of negative clamper. **(06 Marks)**

b. Derive an expression for the stability factor $S_{(VBE)}$ and $S_{(ICO)}$ for fixed bias circuit. **(06 Marks)**

c. Determine the DC bias voltage V_{CE} and the current I_C for the voltage divider bias shown in Fig.Q1(c). Given $\beta = 160$ and assume silicon transistor.

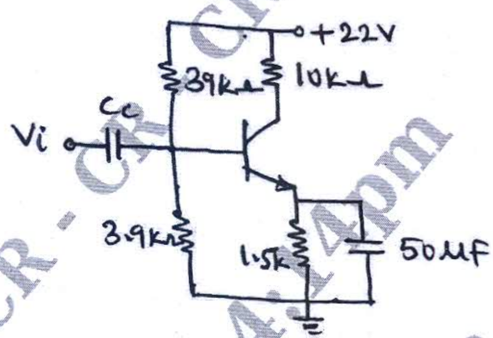

Fig.Q1(c) **(08 Marks)**

OR

2 a. For the clipper circuit shown in Fig.Q2(a), the input is 50 sin ωt. Draw the transfer characteristics and input-output waveforms, assuming ideal diodes.

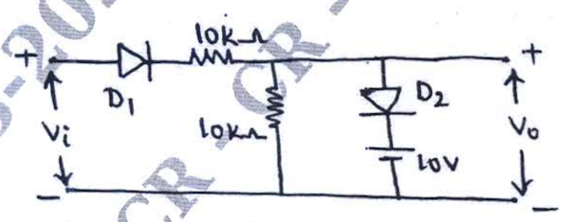

Fig.Q2(a) **(10 Marks)**

b. Design an emitter stabilized circuit using the following data : $I_{CQ} = \frac{1}{2}I_{C(sat)}$, $V_{CE} = \frac{1}{2}V_{CC}$, $V_{CC} = 2V$, $I_{Csat)} = 10mA$, $\beta = 120$ and $R_C = 4R_E$. **(10 Marks)**

Module-2

3 a. Define h-parameters. Draw the h-parameter model of a transistor in CE mode. **(06 Marks)**

b. Derive the expressions for A_I, A_V, R_i and R_o for CE amplifier using complete hybrid equivalent model. **(10 Marks)**

c. State and prove Miller's theorem. **(04 Marks)**

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

4 a. Derive an expression for input impedance, output impedance and voltage gain of an emitter – follower configuration using approximate hybrid equivalent model. **(10 Marks)**

b. For the circuit shown in Fig.Q4(b). Use Miller's theorem calculate A_I, R_i, A_V and R_i'. Given $h_{ie} = 1100\Omega$, $h_{fe} = 50$, $h_{oe} = \frac{1}{40}k\Omega$ and $h_{re} = 2.5 \times 10^{-4}$.

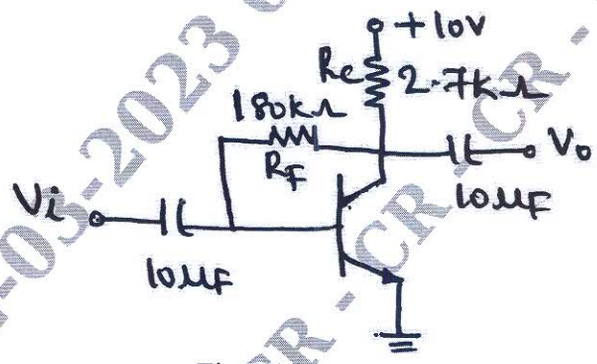

Fig.Q4(b) **(10 Marks)**

Module-3

5 a. Draw the block diagram of two stage cascade amplifier and explain its advantages. **(06 Marks)**

b. Draw a feedback amplifier in block diagram form. Identify each block and explain its function. **(08 Marks)**

c. An amplifier with a 1kΩ input resistance and a 50kΩ output resistance, has a voltage gain of 40. The amplifier is now modified to provide a 10% negative voltage feedback in series with the input. Calculate :

i) The voltage gain with feedback
ii) The input resistance with feedback
iii) The output resistance with feedback. **(06 Marks)**

OR

6 a. Prove that AC voltage gain is approximately unity for a Dralington emitter follower. Use h-parameter model. **(10 Marks)**

b. List the four types of feedback connections. Write the block diagram for each and explain. **(10 Marks)**

Module-4

7 a. Discuss the different types of power amplifiers. **(05 Marks)**

b. Explain the characteristics of a crystal, with a neat diagram explain the crystal oscillator in parallel resonant circuits. **(08 Marks)**

c. A class B amplifier provides a 18V peak signal to a 16Ω load and a power supply of $V_{CC} = 28V$. Determine the input power, output power and circuit efficiency. **(07 Marks)**

OR

8 a. With the help of a circuit diagram, explain the working of transformer – coupled class-B push-pull amplifier. **(10 Marks)**

b. Draw and explain the Wein bridge oscillators. Derive the frequency of oscillations. **(10 Marks)**

Module-5

9 a. Discuss the difference between JFET and MOSFET. **(05 Marks)**

b. Draw the JFET amplifier using fixed bias configuration. Derive $_I$, t_0 and A_v using small signal model. **(10 Marks)**

c. A JFET has $g_m = 5mv$ at $V_{GS} = -1V$. Find I_{DSS} if pinch-off voltage $V_p = -2.0V$ **(05 Marks)**

OR

10 a. Explain the basic operation and characteristics of n-channel depletion type MOSFET. **(10 Marks)**

b. For the JFET amplifier shown in Fig.Q10(b). Calculate g_m, r_d, z_i, z_0 and A_v. Given $I_{DSS} = 5mA$, $V_p = -6V$ and $Y_{Os} = 40\mu s$.

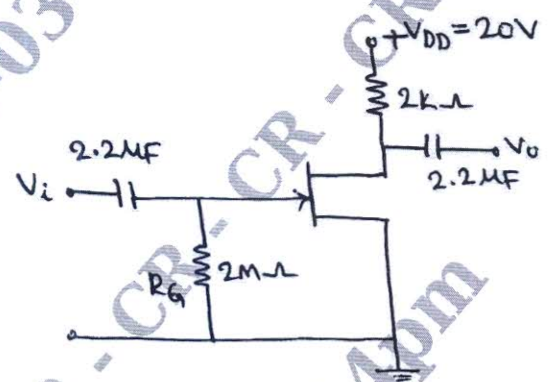

Fig.Q10(b) **(10 Marks)**

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