CBCS SCHEME

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18EC62

Sixth Semester B.E. Degree Examination, Jan./Feb. 2023
Embedded Systems

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat diagram, explain the architecture of ARM crotox M_3 processor. **(10 Marks)**

b. Explain two stack model and reset sequence of ARM cortex M_3. **(10 Marks)**

OR

2 a. With the help of neat diagram, explain operation modes and privilege levels of cortex M_3. **(10 Marks)**

b. With the help of register bit format, explain XPSR register in detail. **(06 Marks)**

c. Explain the function of special registers PRIMASK, BASEPRI, CONTROL, FAULTMASK. **(04 Marks)**

Module-2

3 a. Explain the operation of following instructions with syntax and an example for each:
i) ADD.W ii) LDMIA iii) BEQ iv) LSR v) IF-THEN. **(10 Marks)**

b. Explain different rotate and reverse instructions of cortex M_3 with example for each. **(10 Marks)**

OR

4 a. Explain SSAT and USAT saturation instructions with an example. **(05 Marks)**

b. Write an assembly language program to multiply two numbers. **(05 Marks)**

c. With a neat diagram, explain the CMSIS organization, operation, benefits and disadvantages. **(10 Marks)**

Module-3

5 a. Define embedded system. Classify an embedded system based on i) Generation ii) Complexity iii) Triggering. **(10 Marks)**

b. Explain the purpose of an embedded system. **(06 Marks)**

c. Mention the application of an embedded system in different domains. **(04 Marks)**

OR

6 a. Differentiate between RISC and CISC. **(06 Marks)**

b. With a neat interface diagram, explain the onboard I^2C communication bus. **(08 Marks)**

c. Explain the following:
i) Optocoupler ii) Zig-bee iii) Wi-fi, **(06 Marks)**

Module-4

7 a. Define and explain operational and non operational quality attributes of an embedded system. **(10 Marks)**

b. With a block diagram, explain the role of different components of washing machine. **(07 Marks)**

c. Explain super loop based approach for embedded firmware design. **(03 Marks)**

OR

8 a. With a neat flow diagram, explain high level language source file to machine language conversion. **(06 Marks)**

b. Compare DFG and CDFG models with an example. **(06 Marks)**

c. With the help of FSM model, explain the design and operation of automatic seat belt warning system. **(08 Marks)**

Module-5

9 a. Define the term operating system, with a neat diagram, explain the operating system architecture. **(07 Marks)**

b. Define process, explain in detail the structure, memory organization and state transitions of the process/task. **(07 Marks)**

c. Three processes with process IDs P_1, P_2, P_3 with estimated completion time 10, 5, 7 miliseconds respectively enters the ready queue together. A new process P_4 with estimated completion time 2ms enters the ready queue after 2ms. Calculate the waiting time for all the processes and the turn around time for all the processes. Also, calculate the average waiting time and turn around time. Algorithm used is SJF (Shortest Job First) based preemptive scheduling. Assume all the process contain only CPU operation and no I/O operation are involved. **(06 Marks)**

OR

10 a. Explain the concept of 'deadlock' with a neat diagram. Mention the different conditions which favors a deadlock situation. **(08 Marks)**

b. Write a block schematic of IDE environment for embedded system design and explain their functions in brief. **(08 Marks)**

c. Write a note on IAP [In Application Programming] and in system programming. **(04 Marks)**

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