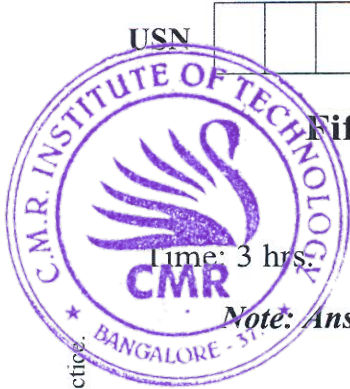


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Fifth Semester B.E. Degree Examination, Jan./Feb. 2023 Verilog HDL

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Sketch the typical digital design flow and identify the design levels and process blocks in the design flow. (10 Marks)
- b. With an example, contrast the two design methodologies used for digital design. (10 Marks)

OR

- 2 a. Explain the importance and popularity of verilog HDL. (10 Marks)
- b. Define module and instances. Describe four levels of abstractions used in verilog HDL to represent the same module. (10 Marks)

Module-2

- 3 a. With examples, illustrate the use of following data types:
i) Nets ii) Registers iii) Vectors iv) Parameters v) Strings. (10 Marks)
- b. With a neat sketch of port connection rules of a module instance, examine the legality of connection between ports. (06 Marks)
- c. With example, illustrate the use of i) Define ii) Include compiler directives. (04 Marks)

OR

- 4 a. Specify and elaborate the two methods of connecting ports to external signals with an example. (10 Marks)
- b. With a neat block diagram, outline the basic components of a verilog module. (06 Marks)
- c. Identify distinct components for the module shown below in Fig.Q.4(c). (04 Marks)

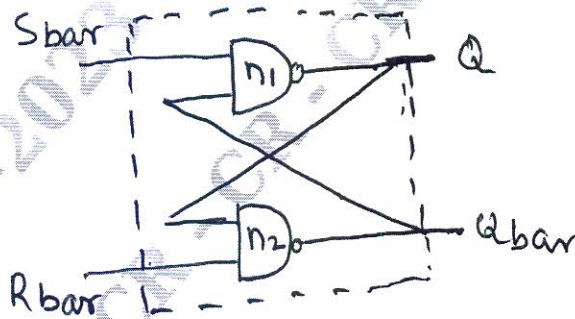


Fig.Q.4(c)

Module-3

- 5 a. By considering 4 – to – 1 multiplexer, illustrate the design of gate-level digital circuits. Also write stimulus code for the same. (10 Marks)
- b. Implement the following function in verilog $f = a.b + c.d$. Include 2 unit delay for AND gate and 1 unit for OR gate and also write the stimulus for the design block. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 6 a. Illustrate the use of conditional operator by writing a verilog dataflow description and stimulus code for 4 – to – 1 multiplexer. (10 Marks)
- b. With relevant examples, differentiate between following operators used in verilog HDL.
- Logical and reduction operators.
 - Concatenation and replication operators.
 - Logical equality and case equality operator. (10 Marks)

Module-4

- 7 a. Describe the use of following loop statements with examples:
i) repeat ii) forever iii) while iv) for. (10 Marks)
- b. Write a verilog behavior program for 8:1 multiplexer using case statement and also write test bench code to verify the same. (10 Marks)

OR

- 8 a. With examples, illustrate the use of event based timing controls in verilog HDL. (10 Marks)
- b. With illustration, differentiate between sequential and parallel blocks. (10 Marks)

Module-5

- 9 a. Describe the capabilities and short coming in VHDL. (06 Marks)
- b. Identify the errors in the following entity declaration of a 4-bit full adder:
entity full adder
Port (a, b : in std-logic (3 to 0);
c : in std-logic;
sum : out std-logic-vector (3 down to 0);
carry : out std-logic);
end full-adder. (04 Marks)
- c. Describe the following VHDL data types: i) Enumerated ii) Physical iii) Real
iv) Record v) Integer. (10 Marks)

OR

- 10 a. Explain the relationship between a design entity and its entity declaration and architecture body in VHDL. (10 Marks)
- b. Write a VHDL code for half adder in
i) Data flow description
ii) Structural description. (10 Marks)

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