CBCS SCHEME

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18EC72

Seventh Semester B.E. Degree Examination, June/July 2023
VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Implement a 4 : 1 multiplexer using :
i) Transmission gate
ii) Tristate inverters **(08 Marks)**

b. Realize CMOS compound gate for the function : $Y = \overline{D + A(B+C)}$. **(04 Marks)**

c. With necessary circuit diagram and timing diagram explain the operation of positive edge triggered D flip-flop. **(08 Marks)**

OR

2 a. Draw the circuit diagram of a CMOS inverter and its DC transfer characteristics. Explain various region of operation and indicate the voltage levels. Derive the equation for switching threshold. **(10 Marks)**

b. Derive the equation for drain current of a MOSFET in non-saturated and saturated region of operation. **(06 Marks)**

c. Explain the following non-ideal effects of a MOSFET –channel length modulation mobility degradation. **(04 Marks)**

Module-2

3 a. With necessary diagrams explain CMOS n-well fabrication process. **(12 Marks)**

b. Draw the layout of $Y = \overline{ABC + D}$ and estimate the area. **(08 Marks)**

OR

4 a. With necessary diagrams explain lambda based design rules for wires, contact cuts and transistors. **(08 Marks)**

b. Explain MOSFET capacitances in three different regions of operation with necessary diagrams and equations. **(06 Marks)**

c. What is Scaling? Compute drain current, power, current density, power density, Cox for constant field scaling. **(06 Marks)**

Module-3

5 a. Explain the RC delay model to compute the delay of the logic circuit. Also calculate the delay of unit size inverter driving another unit size inverter. **(08 Marks)**

b. With necessary circuit example explain :
i) Pseudo nMOS
ii) Ganged CMOS. **(06 Marks)**

c. Explain the following CMOS optimization techniques with necessary examples :
i) Input ordering
ii) Asymmetric gates. **(06 Marks)**

OR

6 a. Analyze the three input NAND gate using Elmore's delay and compute the falling and rising propagation delays if the output is loaded with 'h' identical gates. **(08 Marks)**

b. Compute and compare the logical effort and parasitic delay of the following gates with the help of schematic diagram :
i) 2 input NOR gate
ii) Input NAND gate. **(06 Marks)**

c. Explain Cascade voltage switch logic (CVSL) implement two input OR/NOR gate using CVSL. **(06 Marks)**

Module-4

7 a. Compute the output voltage V_{out} in the following pass transistor circuits. Assume $V_{tn} = 0.7V$.

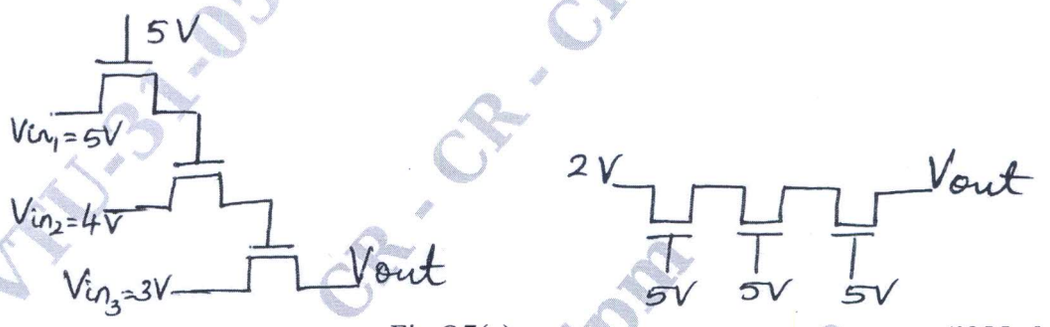

Fig.Q7(a) **(08 Marks)**

b. With necessary diagrams and equations explain charge storage and charge leakage in dynamic logic. **(06 Marks)**

c. With necessary circuit diagrams explain resettable latches with :
i) synchronous reset ii) asynchronous reset. **(06 Marks)**

OR

8 a. Explain dynamic logic with an example. Also explain the advantage and limitations of dynamic logic. **(08 Marks)**

b. With necessary circuit diagram explain 3 bit dynamic shift register with enhancement load (radio less). **(08 Marks)**

c. Explain dynamic synchronous CMOS transmission gate logic with necessary diagrams. **(04 Marks)**

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Module-5

9 a. With necessary circuit diagram explain the operation of four transistor DRAM cell. **(06 Marks)**

b. Explain the terms : i) controllability ii) obsevability iii) repeatability iv) survivability. **(08 Marks)**

c. Explain full CMOS SRAM cell with necessary circuit topology. **(06 Marks)**

OR

10 a. Explain CMOS bridging fault with necessary example. **(06 Marks)**

b. What is a fault model? Explain stuck at fault model with examples. **(08 Marks)**

c. Draw the circuit of 3 bit BILBO register and explain. **(06 Marks)**

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