CBCS SCHEME

USN | | | | | | | | | |

15TE73

Seventh Semester B.E. Degree Examination, June/July 2023

CMOS VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the DC transfer characteristics of complementary CMOS inverter and mark all the regions of operation with necessary expressions for V_{out} in each region. **(07 Marks)**

b. Describe with neat diagram, the P-well fabrication process. **(06 Marks)**

c. Compare CMOS and Bipolar technology. **(03 Marks)**

OR

2 a. Explain nMOS fabrication process. **(07 Marks)**

b. Discuss :

i) Channel length modulation

ii) Body effect. **(06 Marks)**

c. Demonstrate the operation of tristate inverter with neat diagram. **(03 Marks)**

Module-2

3 a. Obtain the expression for sheet resistance and identify the concept applied to MOS transistors (for 5 mm technology). **(06 Marks)**

b. What are design rules? Explain λ based design rules for polysilicon, diffusion and transistors. **(06 Marks)**

c. Draw a layout for 2 input CMOS NAND gate. **(04 Marks)**

OR

4 a. Derive the expression for Rise time and Fall-time delay of CMOS inverter. **(06 Marks)**

b. Calculate the total area capacitance for the structure given in Fig.Q4(b).

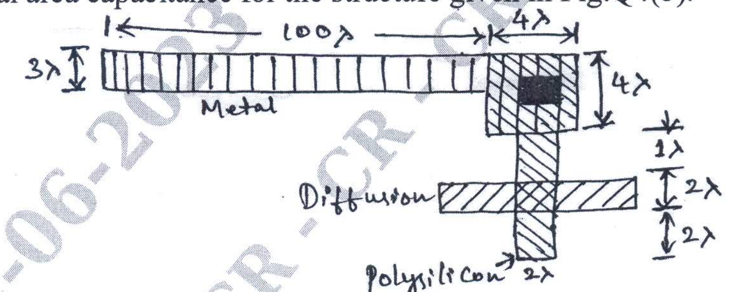

Fig.Q4(b) **(06 Marks)**

c. Write a schematic for CMOS implementation of

(i) $Y = \overline{A(B+C)+DE}$ (ii) $\overline{Y} = AB + CD$ **(04 Marks)**

Module-3

5 a. Determine the scaling factors for the following :

i) Gate capacitance 'C_g'

ii) Gate delay 'T_d'

iii) Saturation current 'Id_{ss}'

iv) Current density 'J'. **(08 Marks)**

b. Explain the design of 4 bit shifter using 4 × 4 crossbar switch. **(08 Marks)**

OR

6 a. Explain 4 bit data path for processor with neat block diagram. (04 Marks)
b. Explain Manchester carry chain. (04 Marks)
c. Explain Carry LookAhead Adder (CLA) and represent the 4 bit block CLA unit. (08 Marks)

Module-4

7 a. Discuss the architectural issues to be followed in the design of VLSI subsystem. (06 Marks)
b. Design a bus arbitration logic for n-line bus. (10 Marks)

OR

8 a. Explain the generic structure of an FPGA fabric. (08 Marks)
b. Explain the two major phases placement and routing in physical design. (08 Marks)

Module-5

9 a. Discuss the system timing considerations in designing memory subsystem. (05 Marks)
b. Explain the Read and write operation in 3T DRAM cell. (05 Marks)
c. Explain Design for manufacturability. (06 Marks)

OR

10 a. Discuss the logic verification at different level of abstraction and its principles. (06 Marks)
b. Explain the operation of pseudo static RAM cell. (05 Marks)
c. Explain 4T RAM cell with its read and write operation. (05 Marks)

* * * * *