USN | | | | | | | | | | |

CMRIT

Internal Assessment Test 1 – Dec 2022

Sub:	Analog and Digital Electronics					Sub Code:	21CS33	Branch:	CSE
Date:	8/2/23	Duration:	90 mins	Max Marks:	50	Sem / Sec:	3rd semester/A, B, C		OBE

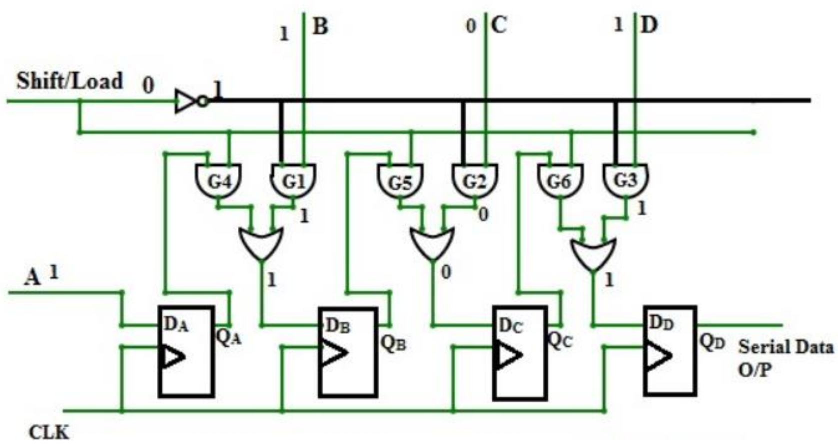
Answer any FIVE FULL Questions	MARKS	CO	RBT
1 a) What is the function of shift/Load signal in PISO shift register.	[2+6+2]	CO4	L1, L2, L3

1 a) What is the function of shift/Load signal in PISO shift register.

Ans- PISO works in two modes one is load and another is shift mode.
In load mode we have the parallel input of the data in which we load the data in each of the flip flop simultaneously. And shift signal helps shifting the data serially from one flip flop to the next one.

b) Design Parallel in serial out shift register.

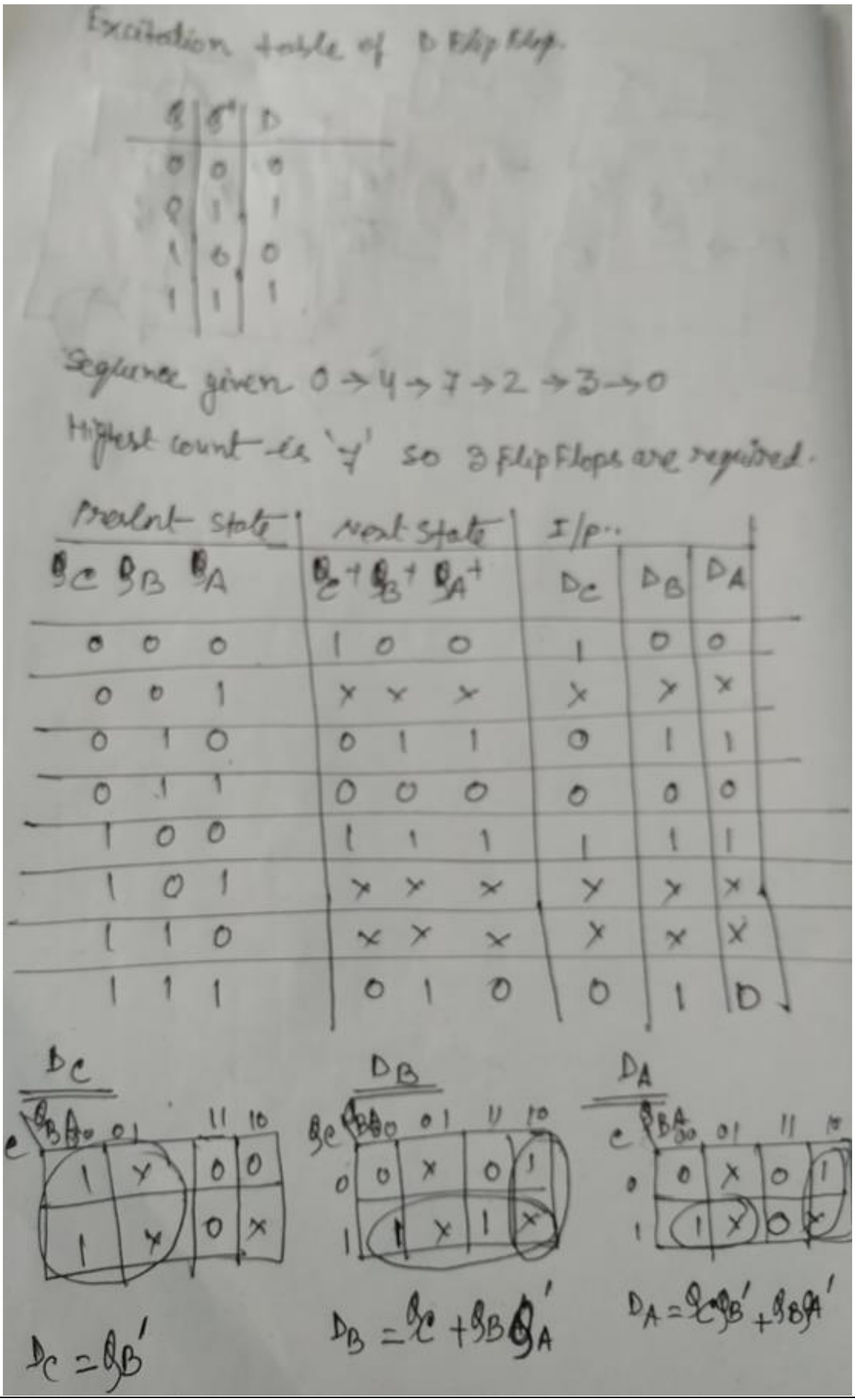
Ans- The PISO shift register circuit diagram is shown below.



This circuit mainly includes 4 D FFs which are connected as per the diagram shown. The CLK i/p signal is connected directly to all the FFs however the i/p data is individually connected to every flip flop.
PISO shift register circuit, the input data is applied to the input pins of the shift registers from DA to DD at the same time. After that, it is read out from the shift register serially 1-bit at a time from input pins on every CLK cycle. Here, one CLK pulse is enough to load the 4-bit of data but four pulses are required to unload all the four bits.
In this parallel input serial output (PISO) shift register circuit, logic gates are used. One control signal (Shift/Load) is used to control the parallel input and serial output. After that, NOT gate outputs are connected

	to 'G1', 'G2', and 'G3', and the other inputs of G1, G2 & G3 are B, C & D. Here, 'A' is directly connected to DA of the first flip flop. The direct control signal is connected to one input of the 'G4', 'G5' & 'G6' and one more input of the 'G4', 'G5' & 'G6' are connected to the outputs of Flip Flops like QA, QB, and QC. The OR gate is connected to the second, third, and fourth Flip Flop's inputs like DB, DC, and DD. All the flip flops are to be connected in a single CLK pulse and the FFs outputs will be in the serial data output. Here, we are choosing the input data as 1101 then A=1, B=1, C=0 & D=1. When the control signal applied to NOT gate is '0' then its o/p will become'1' and 'G1, 'G2' & 'G3' will enable, and 'G4', 'G5' & 'G6' will disable. So, all the inputs are loaded and after that OR gates are also enabled and the data is to be loaded to the input of each Flip Flop. Now we are applying the control signal '1 to NOT gate then the output of this gate will become '0' then G4, G5 & G6 are enabled. Once the CLK pulse is applied to FFs, then the data '1101' is shifted to the right side from one OR gate to the other. c)How many clock pulses are required to load a 4-bit data in SIPO register and how many clock pulses are required to transfer the data to an output register? Ans-4 clock pulses are required to load a 4-bit data in SIPO register and 4 clock pulses are required to transfer the data to an output register			
2	Design a synchronous counter using D flip-flops which counts in the following sequence. 0 → 4 → 7 → 2 → 3 → 0.	[10]	CO4	L2, L3

Ans-



Excitation table of D Flip Flop.

Q	Q+	D
0	0	0
0	1	1
1	0	0
1	1	1

Sequence given 0 → 4 → 7 → 2 → 3 → 0

Highest count is '7' so 3 flip flops are required.

Present state			Next state			I/p		
Q_C	Q_B	Q_A	Q_C^+	Q_B^+	Q_A^+	D_C	D_B	D_A
0	0	0	1	0	0	1	0	0
0	0	1	x	x	x	x	x	x
0	1	0	0	1	1	0	1	1
0	1	1	0	0	0	0	0	0
1	0	0	1	1	1	1	1	1
1	0	1	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x
1	1	1	0	1	0	0	1	0

D_C

Q_C \ Q_BQ_A	00	01	11	10
0	1	X	0	0
1	1	X	0	X

$D_C = Q_B'$

D_B

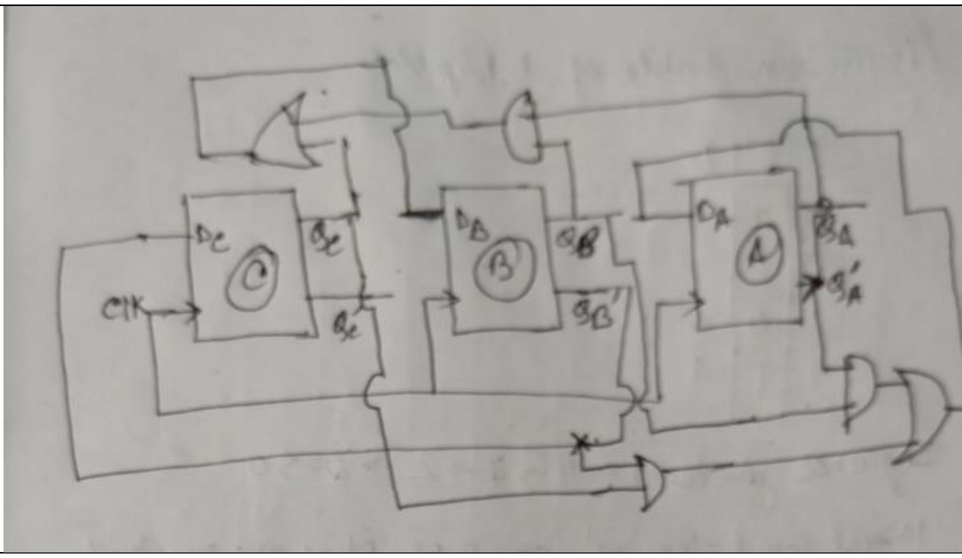
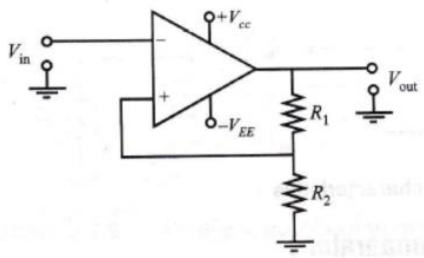
Q_C \ Q_BQ_A	00	01	11	10
0	0	X	0	1
1	1	X	1	X

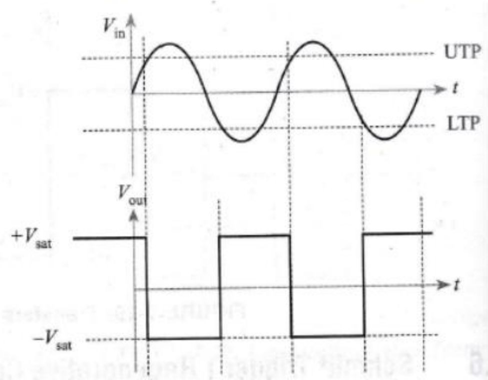
$D_B = Q_C + Q_B Q_A'$

D_A

Q_C \ Q_BQ_A	00	01	11	10
0	0	X	0	1
1	1	X	0	X

$D_A = Q_C Q_B' + Q_B Q_A'$

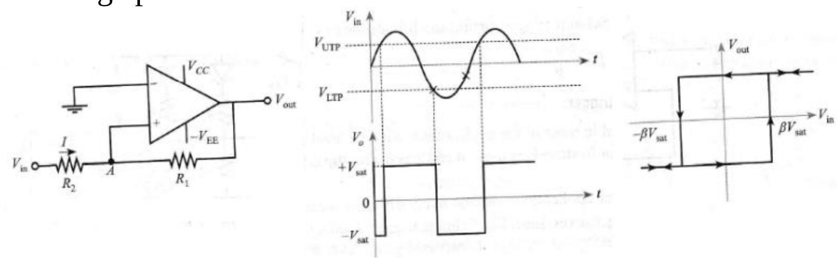
<table>
<tr><td></td><td>
</td><td></td><td></td><td></td></tr>
<tr><td>3</td><td>With the help of neat circuit diagram and waveform, explain the working principle of Schmitt Trigger circuit.
Ans-
<u>Inverting Schmitt Trigger:</u>
The input voltage V_{in} is applied to the inverting input terminal and the feedback voltage goes to the non-inverting terminal. This means, the circuit uses positive voltage feedback (i.e., feedback voltage aids the input voltage).
If the input voltage at the inverting terminal is slightly positive than feedback voltage at the non-inverting terminal, the output voltage will be negative (negative saturation, $-V_{sat}$); and if the input voltage more negative than the reference feedback voltage, the output will be positive (positive saturation, $+V_{sat}$).




Hence, the voltage at the output switches from $+V_{sat}$ to $-V_{sat}$ or vice-versa; are called Upper Trigger Point (UTP) and Lower Trigger Point (LTP). The difference between two trigger points is called Hysteresis.
The upper and lower trigger points can be written as;
$$UTP = \frac{R_2}{(R_1+R_2)} e\, V_{sat} \qquad LTP = \frac{R_2}{(R_1+R_2)} (-V_{sat})$$
$$V_{hys} = UTP - LTP = \frac{R_2}{(R_1+R_2)} e\, V_{sat} - \frac{R_2}{(R_1+R_2)} e\, (-V_{sat}) = 2\left(\frac{R2}{R_1+R_2}\right) V_{sat} = 2\beta V_{sat}$$
$$\beta = \frac{R2}{R_1+R_2}$$</td><td>[10]</td><td>CO1</td><td>L1, L2</td></tr>
</table>

<table>
<tr>
<td></td>
<td>

Non-Inverting Schmitt Trigger: The input voltage Vin is applied to the non-inverting input terminal and the feedback voltage also goes to the non-inverting terminal. The inverting terminal is grounded. Initially, assume that the output is in the negative saturation (–Vsat). Then the feedback voltage is also negative. This feedback voltage will hold the output in negative saturation, until the input voltage becomes positive enough to make voltage positive.



Let V_A is the voltage at point A. Hence, $V_A = IR_2$.

Since no current passes through the Op-Amp, entire current flows through R_2.

Therefore, $I = \frac{V_0}{R_1} = \frac{+V_{sat}}{R_1}$

When V_{in} becomes positive and its magnitude becomes greater than $(R_2/R_1)V_{sat}$, then the output switches to $+V_{sat}$. Therefore, the UTP at which the output switches to $+V_{sat}$ is given by;

$$UTP = \frac{R_2 V_{sat}}{R_1}$$

Similarly, when V_{in} becomes negative and its magnitude becomes greater than $(R_2/R_1)V_{sat}$, then the output switches to $-V_{sat}$. Therefore, the LTP at which the output switches to $-V_{sat}$ is given by;

$$UTP = -\frac{R_2 V_{sat}}{R_1}$$

$$V_{hys} = UTP - LTP = 2\left(\frac{R2}{R_1}\right)V_{sat} = 2\beta V_{sat}$$

$$\beta = \frac{R2}{R_1}$$

</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>a) What is the difference between active filter and passive filter.</td>
<td>[4+6]</td>
<td>CO1</td>
<td>L1, L2</td>
</tr>
</table>

...arison between active filter and passive filters

S.No	Active filters	Passive filters
1	Filters with components such as operational amplifiers, transistors or other active elements are known as active filters.	Filters with only components like R, L and C are known as passive filters
2	Active filters require an external power supply for operation. Capable of providing power gain.	Passive filters do not need an external power source for operation. Incapable of providing power gain.
3	Due to feedback loops used for regulating the active components may contribute to oscillation and noise.	Passive filters have a better stability and can withstand large currents.
4	Active filters have frequency limitations due to active elements.	Passive filters have no frequency limitation.
5	Active filter circuits are more compact and less heavy and operate with high speed	Due to presence of inductors, Passive filters are bulky/heavy in nature, they consume more power and operate with low speed
6	Can be fabricated in IC form and mass production making it cheaper.	Difficult to fabricate in IC form and usually designed using discrete components.

b) Design a first order low pass filter with a cut off frequency of 2.2 kHz and with pass band gain of 2 (Assume C=0.01 μF)

$f_h = 2.2\,KHz$

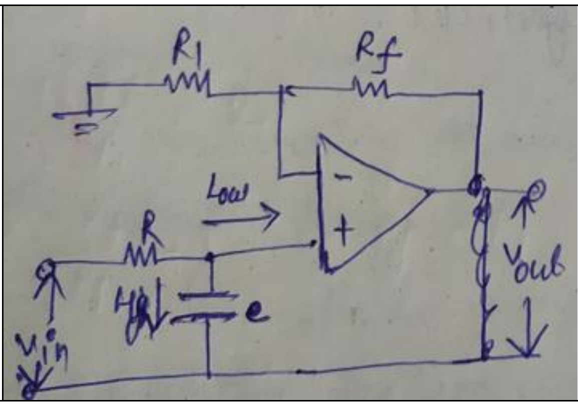
Assume $C = 0.01\,\mu F$ $\qquad f_h = \frac{1}{2\pi RC}$

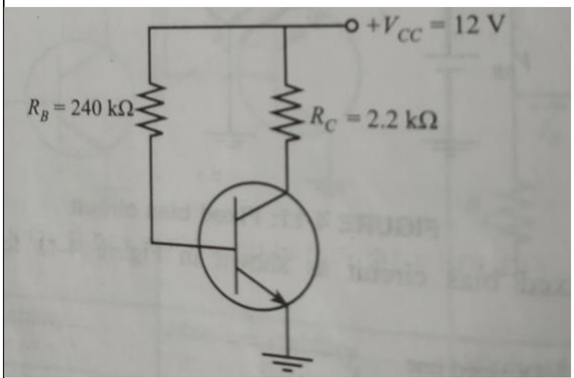
$$\Rightarrow R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi \times 2.2\times10^3 \times 0.01\times10^{-6}}$$

$$= 7.233\,k\Omega$$

$A_F = 1 + \frac{R_f}{R_1}$

$\Rightarrow 2 = 1 + \frac{R_f}{R_1} \Rightarrow \frac{R_f}{R_1} = 1 \Rightarrow R_f = R_1 =$

5	For the circuit shown in figure, a silicon transistor (VBE=0.7 V) with β=50 is used. Draw the dc load line and determine the operating point. 	[10]	CO1	L2, L3

$R_B = 240\ k\Omega, \beta = 50, V_{CC} = 12\ V$

$R_C = 2.2\ k\Omega$. Assume $V_{BE} = 0.7\ V$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{240 \times 10^3}$$

$$\boxed{I_B = 47.08\ \mu A}$$

$$I_C = \beta I_B$$

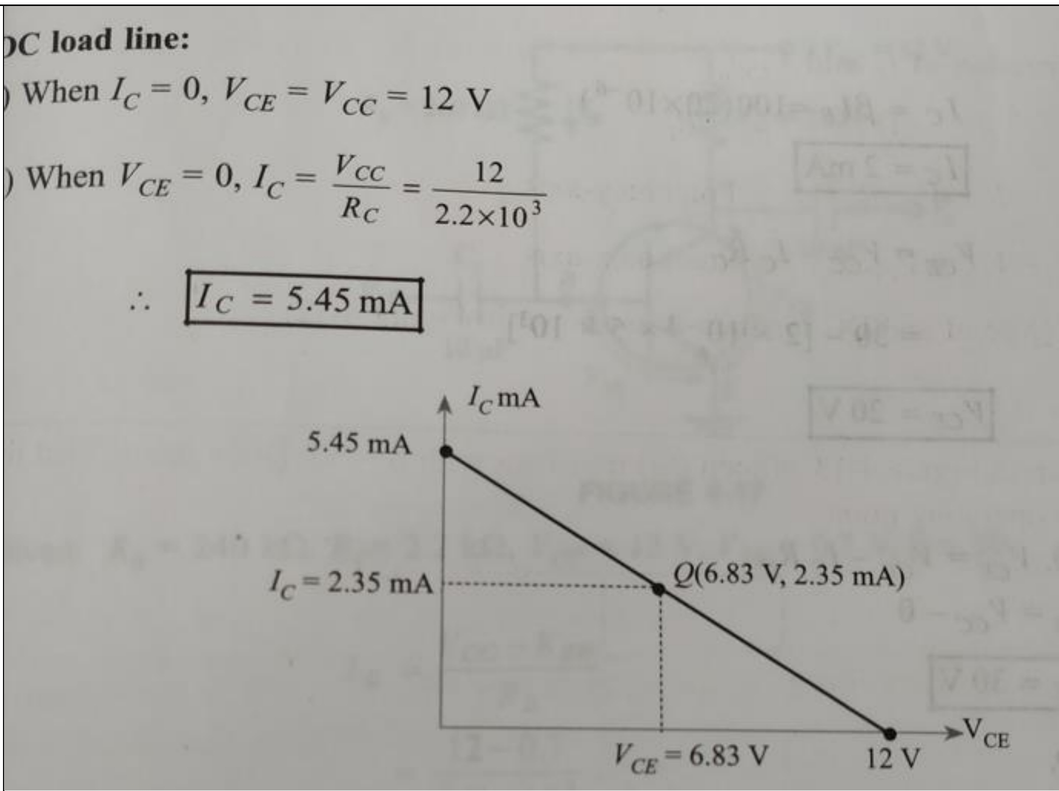
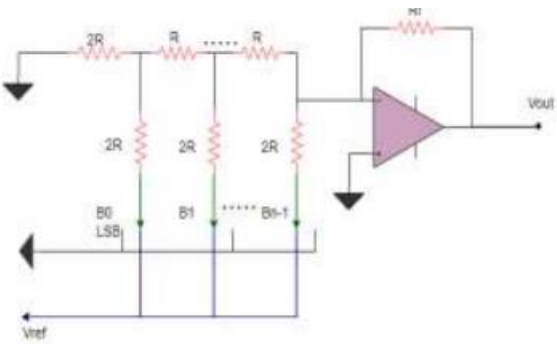
$$= 50 \times 47.08\ \mu A$$

$$\boxed{I_C = 2.35\ mA}$$

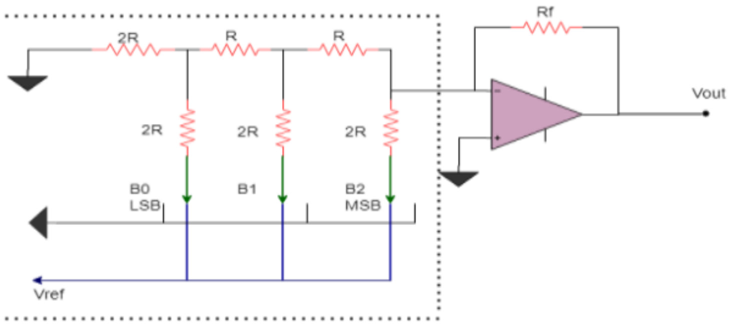
$$V_{CE} = V_{CC} - I_C R_C$$

$$= 12 - \left[2.35 \times 10^{-3} \times 2.2 \times 10^3\right]$$

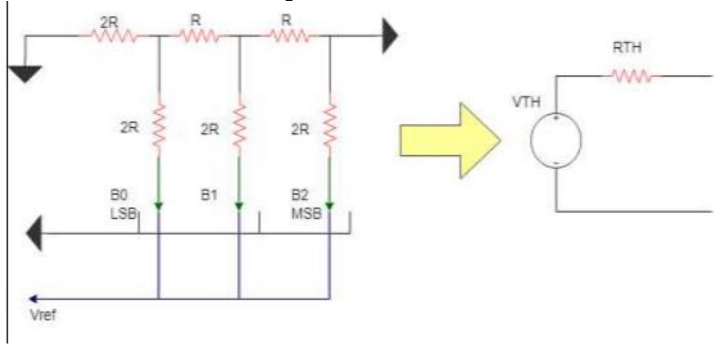
$$\therefore \boxed{V_{CE} = 6.83\ V}$$

	 DC load line:) When $I_C = 0$, $V_{CE} = V_{CC} = 12$ V) When $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C} = \frac{12}{2.2\times10^3}$ $\therefore$ $I_C = 5.45$ mA 			
6	Derive the expression of output voltage of R-2R Ladder circuit. Ans- R-2R configuration is a simple arrangement that consists of parallel and series resistors connected in the cascaded form to an operational amplifier The following diagram shows the R-2R 3-bit ladder DAC. • The leftmost side of the circuitry has the least significant bit i.e B0 whereas B2 which is the most significant bit is connected to the right side of the circuit to the amplifier. • The binary inputs are given through the binary switches. So, when we need a high bit, the concerned bit is connected to the reference voltage and when a low bit is needed, the switch gets connected to the ground potential.  • The ladder arrangement consists of two resistors i.e. a base resistor R and a 2R resistor which is twice the value of the base resistor.	[10]	CO1	L1, L2

R-2R Ladder DAC Analysis with Thevenin Theorem Thevenin's theorem is a technique through which we can obtain an equivalent circuit of the concerned resistance network. A Thevenin circuit consists of a Thevenin resistance and a Thevenin voltage that can be replaced in the circuit and work the same as the original resistance network



RTh is calculated by short-circuiting all the voltage sources and replacing the current sources with open circuits.



When LSB is high

Let us first consider the binary code 001. Its VTh and RTh will be calculated in three stages.

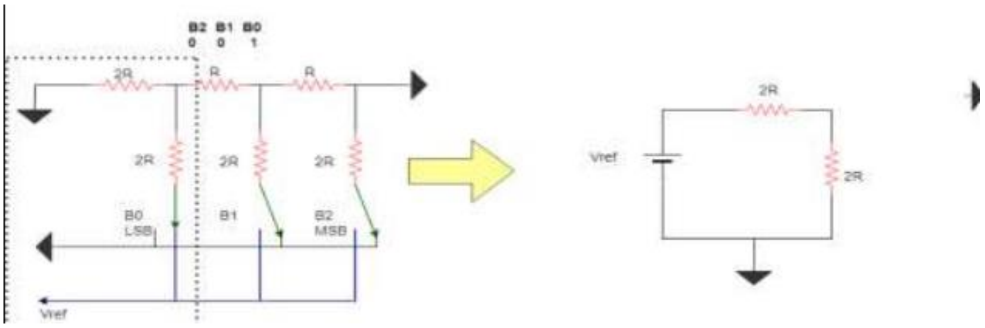
VTh= 2R x Vref / 2R+2R

VTh=Vref / 2

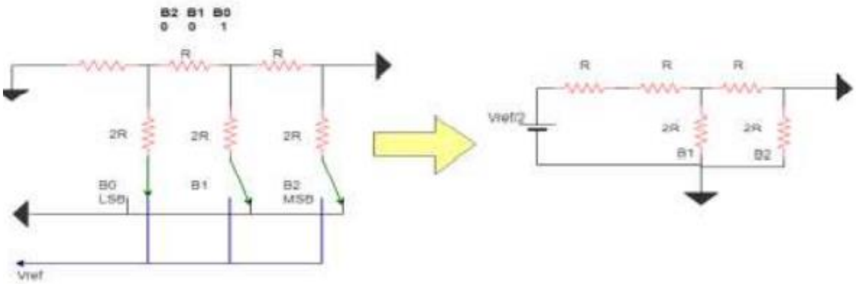
For measuring the Thevenin resistance, short circuit the reference voltage. Two resistances 2R and 2R become parallel to each other.

So, RTh=2R || 2R

RTh=R



Below is the equivalent circuit of the original after simplifying the first stage. The Thevenin equivalent of the first stage is connected in series to the rest of the circuit.



Now, we calculate the Thevenin circuit of the second stage. The dotted block will be solved in the second stage. Two resistors of the same value i.e R are connected in series. So it is replaced by equivalent resistance 2R shown in the given diagram below.

The circuit is again configured to be a voltage divider with reference voltage as Vref/2.

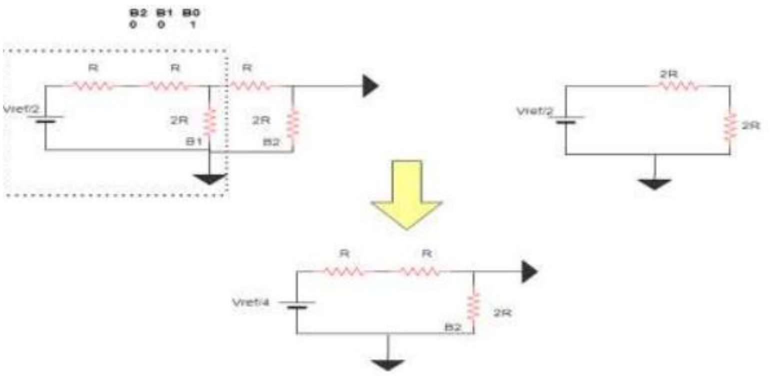
So, VTh= (2R x Vref/2) / 2R+2R

VTh=Vref / 4

for the Thevenin resistance, we consider the voltage source of this block to be zero. It gives the same Thevenin as the previous because of the exact arrangement and we will replace the concerned portion with equivalent Thevenin values

RTh=2R || 2R

RTh=R



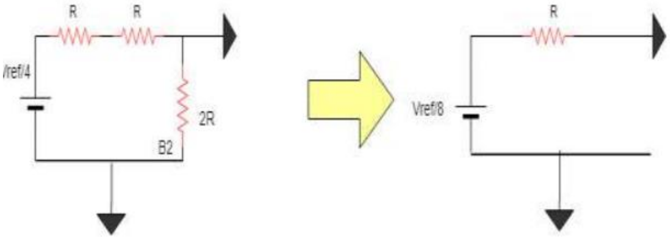
This is the resultant circuit which will be solved in the third stage. The VTh and RTh is as follows:

VTh= (2R x Vref/4) / 2R+2R

VTh=Vref / 8

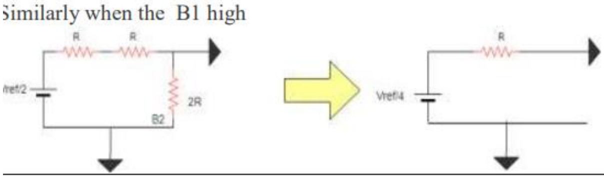
RTh=(R+R) || 2R

RTh=R

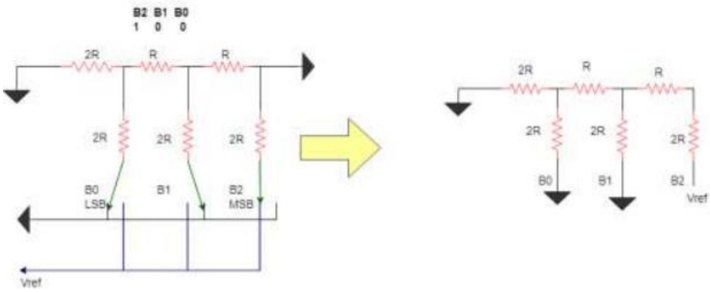


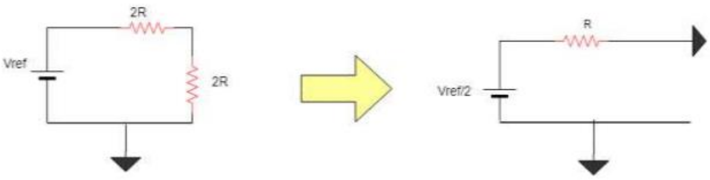
The solution depicts that whenever only B0 is connected to the reference voltage and B2=B1=0, he output voltage of the DAC would be Vref/8.

Similarly when the B1 high



When MSB Bit is high





When all three bits are high

When all 3 bits are connected to the reference voltage, the output voltage will be the superposition of all three voltages.

Vr-2r = (Vref / 2)+(Vref / 4)+(Vref / 8)

Vr-2r = 7Vref / 8 Vr-2r = Vref{B0/2(N) + B0/2(N-1) + B0/2(N-2) + … + B0/22 + B0/21 }

Where N is the number of bits.

Vr-2r is applied to the inverting operational amplifier and the output voltage is measured. The output would be 180 degrees out of phase with the input Vr-2r. The following is the general output voltage equation of R-2R DAC

Vout = -(Rf/R) x Vr-2r

Vout = -(Rf/R){B0/2(N) + B0/2(N-1) + B0/2(N-2) + … + B0/22 + B0/21 }Vref

The gain of the DAC is decided by the (Rf/R) factor..

Faculty Signature CCI Signature HOD Signature

CO PO Mapping

Course Outcomes		Modules covered	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
CO1	Design and analyze application of analog circuits using photo devices, timer IC, power supply and regulator IC, op-amp and basic principles of A/D and D/A conversion circuits and to develop the same.	1	3	3	3	2	2	0	0	0	0	0	0	0	0	2	0	2
CO2	Formulate logical expressions for minimized SOP, POS forms by use of Karnaugh maps, Quine Mc Cluskey method.	2	3	3	3	2	2	0	0	0	0	0	0	0	0	2	0	2
CO3	Design combinational logic circuits using gates, encoders, decoders, multiplexers, demultiplexers, Comparators, arithmetic-logic units and to build simple applications.	3	3	3	3	3	2	0	0	0	0	0	0	0	0	2	0	2
CO4	Understand the use of latches, flip-flops, Switch Contact Bounce Circuits and Various Representation of FLIP-FLOPs and use them in designing, registers and counters.	5	3	3	3	3	2	0	0	0	0	0	0	0	0	2	0	2
CO5	Develop simple HDL programs	4	3	3	3	3	2	0	0	0	0	0	0	0	0	2	0	2

COGNITIVE LEVEL	REVISED BLOOMS TAXONOMY KEYWORDS
L1	List, define, tell, describe, identify, show, label, collect, examine, tabulate, quote, name, who, when, where, etc.
L2	summarize, describe, interpret, contrast, predict, associate, distinguish, estimate, differentiate, discuss, extend
L3	Apply, demonstrate, calculate, complete, illustrate, show, solve, examine, modify, relate, change, classify, experiment, discover.
L4	Analyze, separate, order, explain, connect, classify, arrange, divide, compare, select, explain, infer.
L5	Assess, decide, rank, grade, test, measure, recommend, convince, select, judge, explain, discriminate, support, conclude, compare, summarize.

PROGRAM OUTCOMES (PO), PROGRAM SPECIFIC OUTCOMES (PSO)				CORRELATION LEVELS	
PO1	Engineering knowledge	PO7	Environment and sustainability	0	No Correlation
PO2	Problem analysis	PO8	Ethics	1	Slight/Low
PO3	Design/development of solutions	PO9	Individual and team work	2	Moderate/ Medium

PO4	Conduct investigations of complex problems	PO10	Communication	3	Substantial/ High
PO5	Modern tool usage	PO11	Project management and finance		
PO6	The Engineer and society	PO12	Life-long learning		
PSO1	Develop applications using different stacks of web and programming technologies				
PSO2	Design and develop secure, parallel, distributed, networked, and digital systems				
PSO3	Apply software engineering methods to design, develop, test and manage software systems.				
PSO4	Develop intelligent applications for business and industry