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CMRIT – CMR INSTITUTE OF TECHNOLOGY, BENGALURU. ACCREDITED WITH A+ GRADE BY NAAC

Internal Assessment Test 3 – March 2022

Sub:	Analog and Digital Electronics					Sub Code:	21CS33	Branch:	ISE
Date:	7/2/2023	Duration:	90 min's	Max Marks:	50	Sem/Sec:	III / A, B and C	OBE	

		Answer any FIVE FULL Questions	MARKS	CO	RBT
1		With a block diagram explain the working of 4 bit parallel adder with accumulator	10	CO1	L1
2		Construct Mod 5 counter using SR flip flops	10	CO4	L3
3		With neat sketch, explain the working principle of SISO shift register.	10	CO1	L2
4		List the different types of BJT biasing. Derive the expression for collector emitter voltage (V_{CE}) for voltage divider bias circuit using approximate analysis.	10	CO1	L2
5		With hysteresis characteristics explain the working of Inverting Schmitt Trigger circuit.	10	CO4	L3
6	a	Using a 741 op-amp with a supply of 12V, design inverting Schmitt trigger circuit to have trigger points of ±2V.	5	CO2	L2
	b	Explain the working of Relaxation oscillator with necessary diagrams	5	CO1	L3

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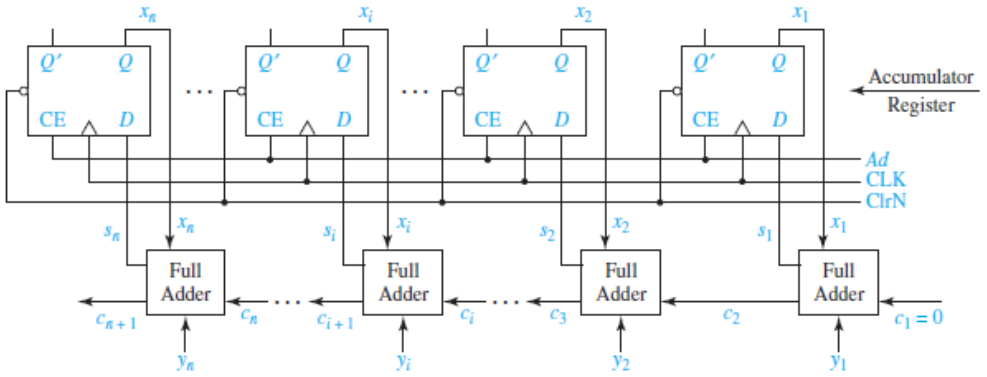
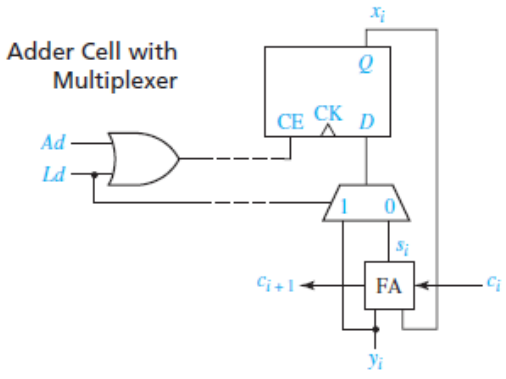
Internal Assessment Test III –February 2023

Sub:	Analog and Digital Electronics					Sub Code:	21CS33	Branch:	ISE	
Date:	07/02/2022	Duration:	90 min's	Max Marks:	50	Sem/Sec:	III / A, B and C			OBE

Answer any FIVE FULL Questions

		MARKS	CO	RBT
1	With a block diagram explain the working of 4 bit parallel adder with Accumulator **Solution:** **Parallel Adder with Accumulator:** In computer circuits, it is frequently desirable to store one number in a register of flip-flops (called an accumulator) and add a second number to it, leaving the result stored in the accumulator. One way to build a parallel adder with an accumulator is to add a register to the adder as shown in the following Figure.  Suppose that the number $X = x_n \ldots x_2 x_1$ is stored in the accumulator. Then, the number $Y = y$ is applied to the full adder inputs, and after the carry has propagated through the adders, the sum of X and Y appears at the adder outputs. An add signal (Ad) is used to load the adder outputs into the accumulator flip-flops on the rising clock edge. If $s_i = 1$, the next state of flip-flop x_i will be 1. If $s = 0$, the next state of flip-flop x_i will be 0.Thus, $x_{i+} = s$, and if $Ad = 1$, the number X in the accumulator is replaced with the sum of X and Y, following the rising edge of the clock. 	10	CO4	L2
2	Construct Mod 5 counter using SR flip flops **Solution:** **1) Excitation table for JK flip flop**	10	CO4	L3

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1

2) Excitation table for counter

Present state			Next state			Flip flop Input					
Q_c	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_a
0	0	0	0	0	1	×	0	0	×	1	×
0	0	1	0	1	0	×	1	1	×	×	1
0	1	0	0	1	1	×	×	×	0	1	×
0	1	1	1	0	0	×	×	×	1	×	1
1	0	0	0	0	0	1	0	0	×	0	×
1	0	1	×	×	×	×	×	×	×	×	×
1	1	0	×	×	×	×	×	×	×	×	×
1	1	1	×	×	×	×	×	×	×	×	×

For J_C

Q_BQ_A / Q_C	00	01	11	10
0	0	0	1	0
1	×	×	×	×

$J_c=Q_BQ_A$

For K_C

Q_BQ_A / Q_C	00	01	11	10
0	×	×	×	×
1	1	×	×	×

$K_C=1$

For J_B

Q_BQ_A / Q_C	00	01	11	10
0	1	×	×	×
1	×	×	×	×

$J_B=QA$

For K_B

Q_BQ_A / Q_C	00	01	11	10
0	×	×	1	0
1	×	×	×	×

$K_B=QA$

For J_A

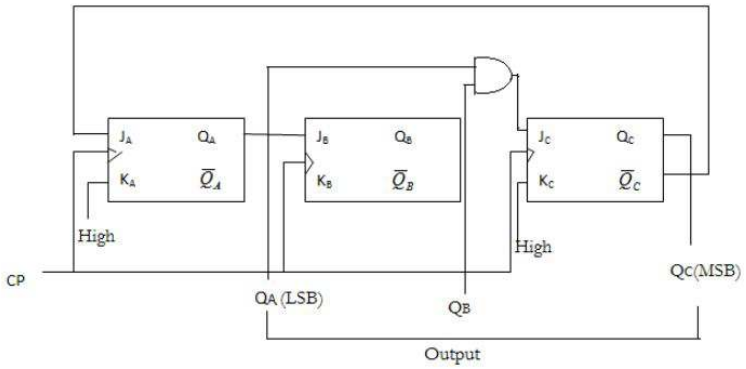
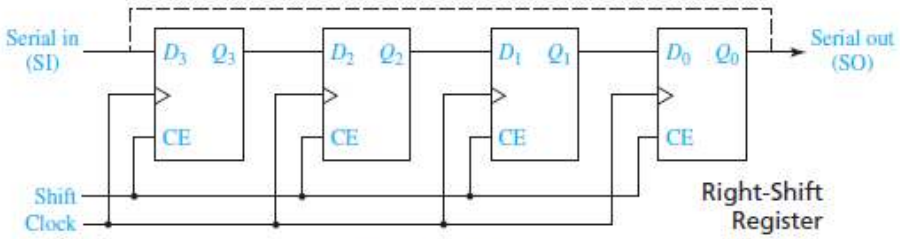
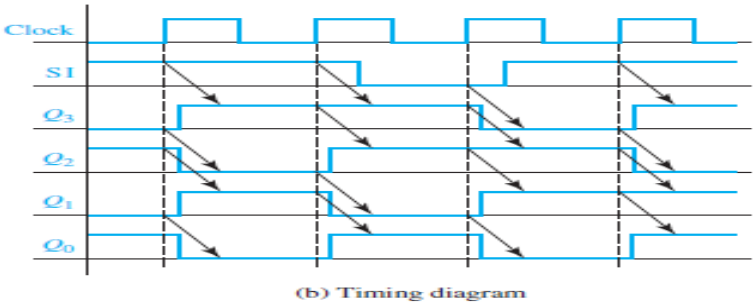
Q_BQ_A / Q_C	00	01	11	10
0	1	×	×	1
1	0	×	×	×

$J_A=Q_c'$

For K_A

Q_BQ_A / Q_C	00	01	11	10
0	×	1	1	×
1	×	×	×	×

$K_A=1$

	Step 5 Logic Diagram 			
3	With neat sketch, explain the working principle of SISO shift register. **Solution:** The following Figure (a) illustrates a 4-bit right-shift register with serial input and output constructed from D flip-flops. When *Shift = 1*, the clock is enabled and shifting occurs on the rising clock edge. When *Shift = 0*, no shifting occurs and the data in the register is unchanged. The serial input (*SI*) is loaded into the first flip-flop (Q3) by the rising edge of the clock. At the same time, the output of the first flip-flop is loaded into the second flip-flop, the output of the second flip-flop is loaded into the third flip-flop, and the output of the third flip-flop is loaded into the last flip-flop. Because of the propagation delay of the flipflops, the output value loaded into each flip-flop is the value before the rising clock edge.  (a) Flip-flop connections Figure (b) illustrates the timing when the shift register initially contains 0101 and the serial input sequence is 1, 1, 0, 1.The sequence of shift register states is 0101, 1010, 1101, 0110, 1011.  (b) Timing diagram	6	CO4	L2
4	List the different types of BJT biasing. Derive the expression for collector emitter voltage (V CE) for voltage divider bias circuit using approximate analysis. **Solution:**	10	CO1	L2

BJT BIASING

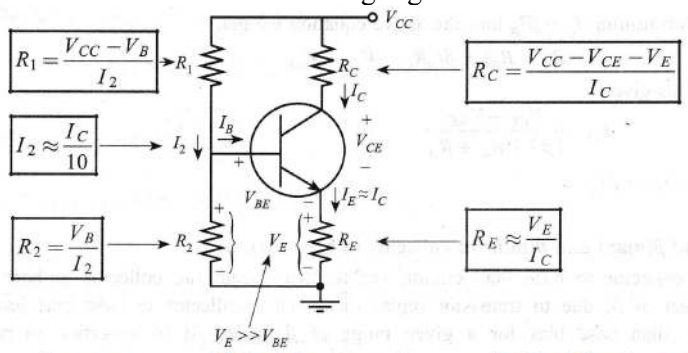
A *transistor* (*Bipolar Junction Transistor-BJT*) is a sandwich of one type of semiconductor (P-type or N-type) between two layers of other type. Transistors are of two types: *p-n-p transistor* and *n-p-n transistor*.

There are three distinct regions (hence, terminals) in a transistor: *Emitter*, *Base*, and *Collector*.

There are mainly three types of biasing a transistor: *Base bias* or *Fixed bias*, *Collector-to-Base bias*, *Voltage-divider bias*.

VOLTAGE DIVIDER (EMITTER CURRENT) BIAS CIRCUIT:

Voltage divider bias is the most stable of the three basic transistor biasing circuits. A voltage divider circuit is shown in the following Figure.



There is an emitter resistor R_E connected in series with Emitter terminal, so that the total dc load in series with the transistor is ($R_C + R_E$). Resistors R_1 and R_2 constitutes a voltage V_B.

Applying KVL to the loop V_{CC}, R_1, and R_2, we get;

$V_{CC} - I_1R_1 - I_2R_2 = 0$ Or, $I_1R_1 + I_2R_2 = V_{CC}$ ---------- (5)

We have; $I_1 = I_2 + I_B$

Voltage divider bias circuits are normally designed to have a voltage divider current I_2 very much greater than transistor base current I_B. i.e., $I_2 >> I_B$. Hence, $I_1 \approx I_2$ ---------- (6)

Using 6 in 5; $I_2R_1 + I_2R_2 = V_{CC}$ i.e., $I_2 (R_1 + R_2) = V_{CC}$ Or, $\boldsymbol{I_2 = (V_{CC}) / (R_1 + R_2)}$

V_B is the voltage across R_2. i.e., $V_B = I_2R_2$ Or, $\boldsymbol{V_B = (V_{CC} * R_2) / (R_1 + R_2)}$

V_E is the voltage across R_E. i.e., $\boldsymbol{V_E = I_ER_E}$

Applying KVL to the base-emitter loop; $V_B - V_{BE} - V_E = 0$ i.e., $\mathbf{V_{BE} = V_B - V_E}$

Or, $V_E = V_B - V_{BE}$ i.e., $I_ER_E = V_B - V_{BE}$ Hence, $\boldsymbol{I_E = (V_B - V_{BE}) / R_E}$

Applying KVL to the collector-emitter loop; $V_{CC} - I_CR_C - V_{CE} - I_CR_E = 0$ $[I_E \approx I_C]$

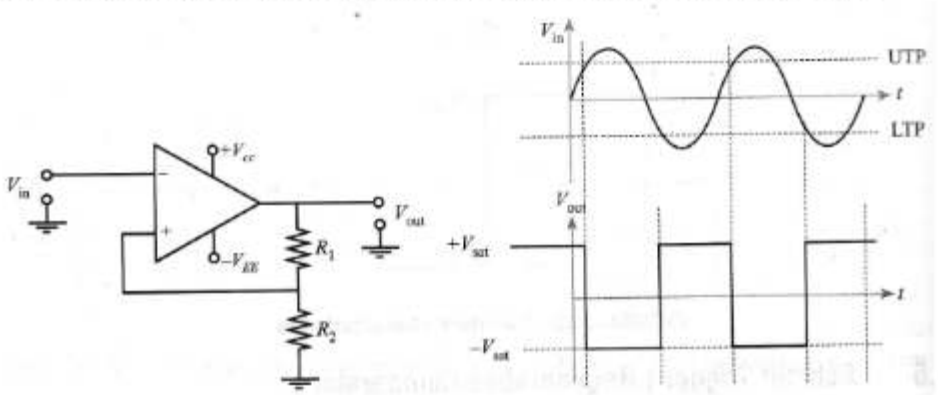
i.e., $\boldsymbol{V_{CE} = V_{CC} - I_C (R_C + R_E)}$

5	With hysteresis characteristics explain the working of Inverting Schmitt Trigger circuit. **Solution:**	10	CO2	L2

Inverting Schmitt Trigger:

The input voltage V_{in} is applied to the inverting input terminal and the feedback voltage goes to the non-inverting terminal. This means, the circuit uses positive voltage feedback (i.e., feedback voltage aids the input voltage).

If the input voltage at the inverting terminal is slightly positive than feedback voltage at the non-inverting terminal, the output voltage will be negative (negative saturation, $-V_{sat}$); and if the input voltage more negative than the reference feedback voltage, the output will be positive (positive saturation, $+V_{sat}$).



Hence, the voltage at the output switches from $+V_{sat}$ to $-V_{sat}$ or vice-versa; are called *Upper Trigger Point (UTP)* and *Lower Trigger Point (LTP)*. The difference between two trigger points is called *Hysteresis*.

The upper and lower trigger points can be written as;

$$UTP = \frac{R_2}{(R_1+R_2)} e\, V_{sat} \qquad LTP = \frac{R_2}{(R_1+R_2)} (-V_{sat})$$

$$V_{hys} = UTP - LTP = \frac{R_2}{(R_1+R_2)} e\, V_{sat} - \frac{R_2}{(R_1+R_2)} e\,(-V_{sat}) = 2\left(\frac{R2}{R_1+R_2}\right) V_{sat} = 2\beta V_{sat}$$

$$\beta = \frac{R2}{R_1+R_2}$$

6 A	Using a 741 op-amp with a supply of 12V, design inverting Schmitt trigger circuit to have trigger points of ±2V.	05	CO2	L3

Solution:

Using a 741 op-amp with a supply of ±12 V, design an inverting schmitt Trigger circuit to have trigger points of ±2 V.

Given: $V_{cc} = \pm 12$ V, LTP = –2 V $C_2 \geq C_{B(max)}$, |LTP| = ±2 V

Let $C_2 = 50\ \mu A$, $V_{R_2} = UTP = +2$ V

$$R_2 = \frac{V_{R2}}{I_2} = \frac{2}{50\times10^{-6}} = 40\ k\Omega$$

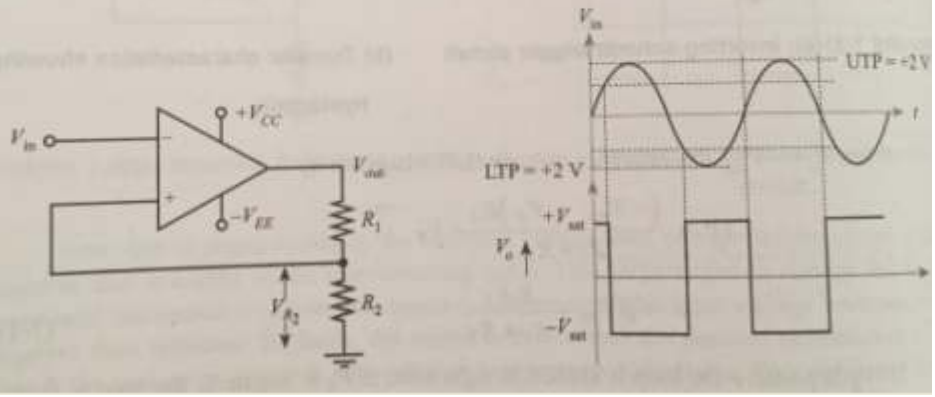
$$R_2 = 40\ k\Omega$$

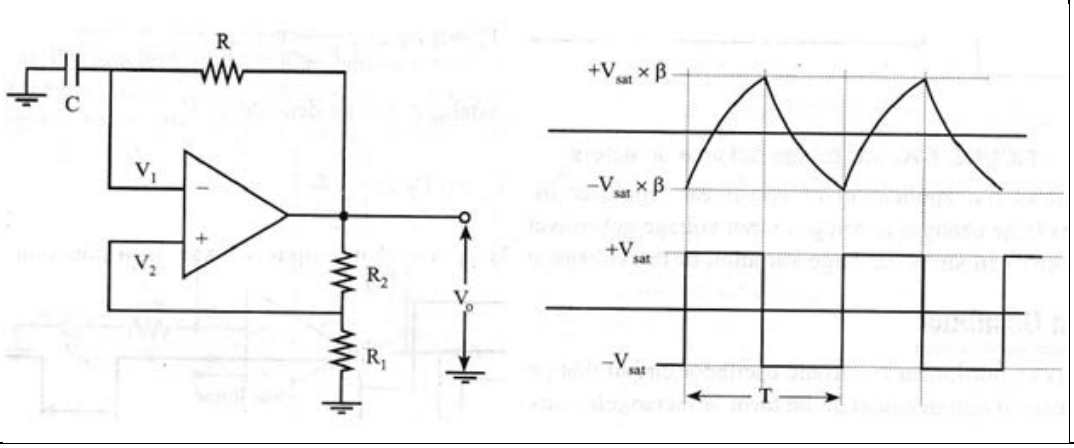
$$R_1 = \frac{V_{0(sat)} - (\text{Trigger voltage})}{C_2}$$

$$R_1 = \frac{(12-1)-2}{50\times10^{-6}} = 180\ \text{k}\Omega \qquad \because V_{sat} = V_{CC} - 1$$

$$R_1 = 180\ \text{k}\Omega$$

Note: Above circuit used only if (UTP) = –|LTP|



6 B	Explain the working of Relaxation oscillator with necessary diagrams. **Solution:** **RELAXATION OSCILLATOR:** Relaxation oscillator is a non-linear electronic oscillator circuit that generates a continuous non-sinusoidal output signal in the form of rectangular wave, triangular wave or a saw-tooth wave. The time period of non-sinusoidal output depends on the charging time of the capacitor connected in the oscillator circuit. The relaxation oscillator basically contains a feedback loop that has a switching device in the form of transistor, relays, operational amplifiers, comparators, or a tunnel diode that charges a capacitor through a resistance till it reaches a threshold level then discharges it again. The following Figure shows the basic circuit of an Op-Amp based relaxation oscillator.  	05	CO2	L2