Analog Electronic Circuits- 21EC34

IAT3 Solution-Feb 2023

Internal Assesment Test - III

Sub:	Analog Electronic Circuits						Code:	21EC34
Date:	07/ 02 / 2023	Duration:	90 mins	Max Marks:	50	Sem: 3rd	Branch:	ECE

Answer Any FIVE FULL Questions

		Marks	OBE	
			CO	RBT
1.	Explain the operation of a Successive -approximation ADC with neat circuit diagram	[10]	CO4	L2
2.	Give the circuit diagram, gain expression and frequency response plots of:- (a) First order Low pass filter (b) Second order Low pass filter (c) Wide band pass filter (d) Narrow band reject filter	[10]	CO4	L2
3.	What are the different turn on methods of SCR? Explain each of them in detail.	[10]	CO5	L2
4	Draw the circuit and frequency response of a second order low pass filter. Derive an expression for the cut off frequency.	[10]	CO4	L3

		Marks	CO	RBT
5.	Explain the static Anode – Cathode characteristics of SCR with circuit diagram and VI characteristics. Define Latching and Holding Currents.	[10]	CO5	L2
6.	Explain the working of UJT and how UJT firing circuit is used for triggering an SCR.	[10]	CO5	L2
7	What is commutation? What are the different types of Commutation? Explain class A commutation in detail.	[10]	CO5	L2
8.	With a neat circuit diagram, explain the working of a Resistance Firing circuit. Determine the trigger angle α for the following specifications:- Ig(min) = 0.1mA, Vg(min) = 0.5 V. The diode is silicon and the peak amplitude of the input is 24 volts. Rv = 100kΩ, Rmin = 10 kΩ.	[10]	CO5	L3

1. SAR ADC

ADC

ADC converts an analog voltage to digital output that best represents the input. ADC are also specified as 8, 10, 12, 16. etc. bit.

Successive-Approximation ADC.

Following figure fig 8.3 shows a successive-approximation type ADC, which uses a comparator, a successive-approximation register, output latches and a DAC.
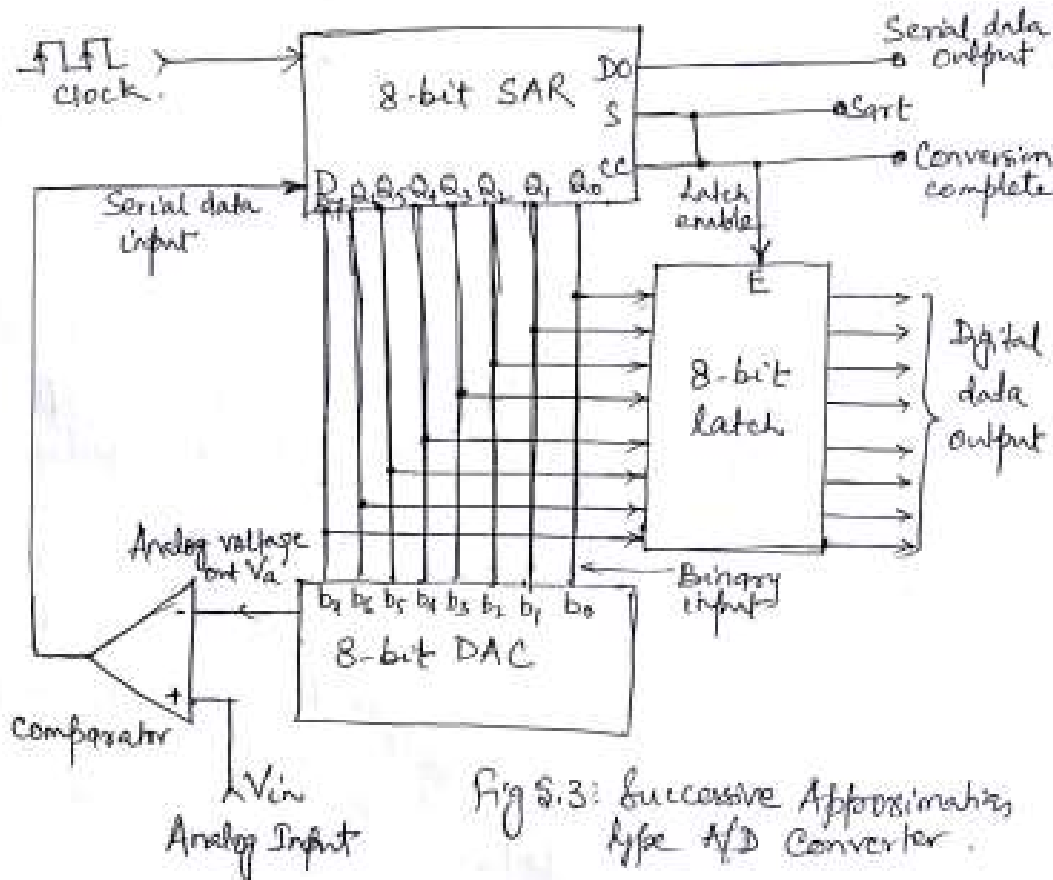

Fig 8.3: Successive Approximation type A/D Converter.

The circuit work as follows:

- At the start of a conversion cycle, the SAR is reset by holding the start (S) signal high.

- On the LOW-to-HIGH transition, the most significant output bit Q_7 of the SAR is set.

- The D/A converter then generates an analog equivalent to the Q_7 bit, which is compared with V_{in}.

- If the comparator output is low, that means DAC output $> V_{in}$ and the SAR will clear its MSB Q_7. On the other hand if comparator output is high, which means DAC output $< V_{in}$, the SAR will keep MSB Q_7 set.

- Similarly depending on the comparator output, the SAR will then either keep or reset bit Q_6, on the next clock pulse LOW-to-high.

- This process is continued until the SAR tries all the bits i.e Q_5, Q_4, Q_3, Q_2, Q_1 and Q_0

- As soon as LSB Q_0 is tried, the SAR forces the conversion complete (CC) signal HIGH to indicate that the parallel output lines contains valid data.

- The CC signal in turns enables the latch, and digital data appear at the output of the latch, which gives the digital representation of the analog voltage Vin.
- For 8 bit SAR type ADC eight clock pulse is required, for 12 bit, 12 clock pulse is required and so on.

- Advantage
  - → High speed
  - → Excellent Resolution.

Example

Clk	B3	B2	B1	B0	VD	VA>VD	Decision	V0	op
	2.5	1.25	0.625	0.3125					
1	1	0	0	0	2.5	No	Reset	0	
2	0	1	0	0	1.25	Yes	Set	1.25	
3	0	1	1	0	1.875	Yes	Set	1.875	
4	0	1	1	1	2.1875	No	Reset	1.875	0110
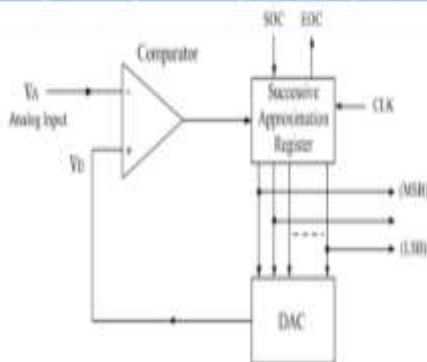
$V_A = 2V$
$V_{ref} = 5$
Step Size = 5/16 = 0.3125

%Error = (2-1.875)*100/2
(0.125*100)/2=6.2%

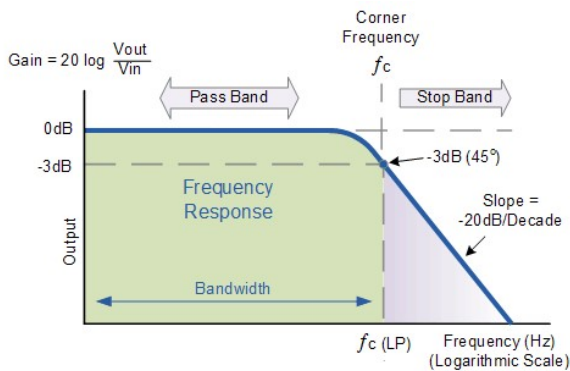2. Give the circuit diagram, gain expression and frequency response plots of:-

(a) First order Low pass filter

(b) Second order Low pass filter

(c) Wide band pass filter

(d) Narrow band reject filter

a) First order Lowpass
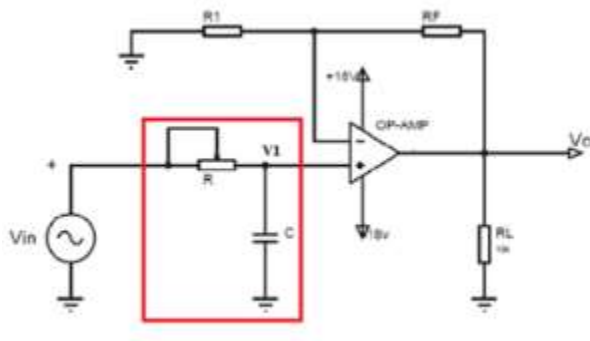
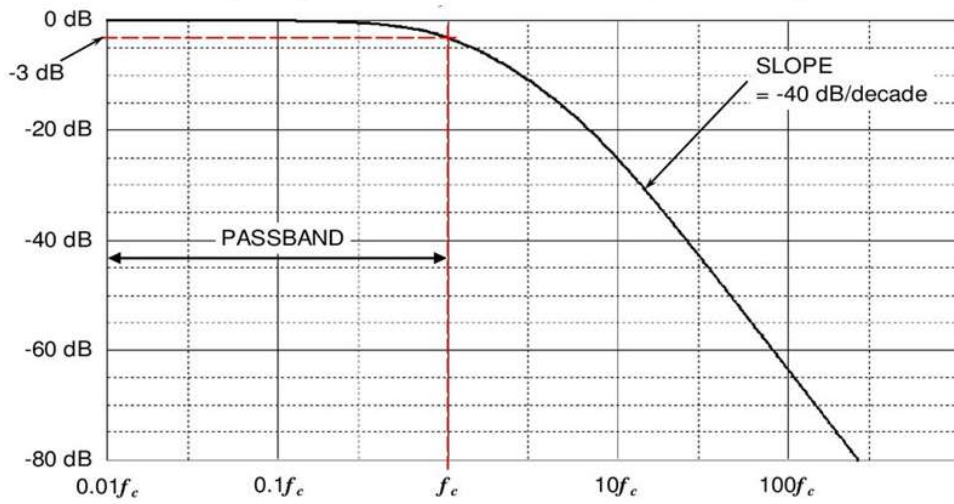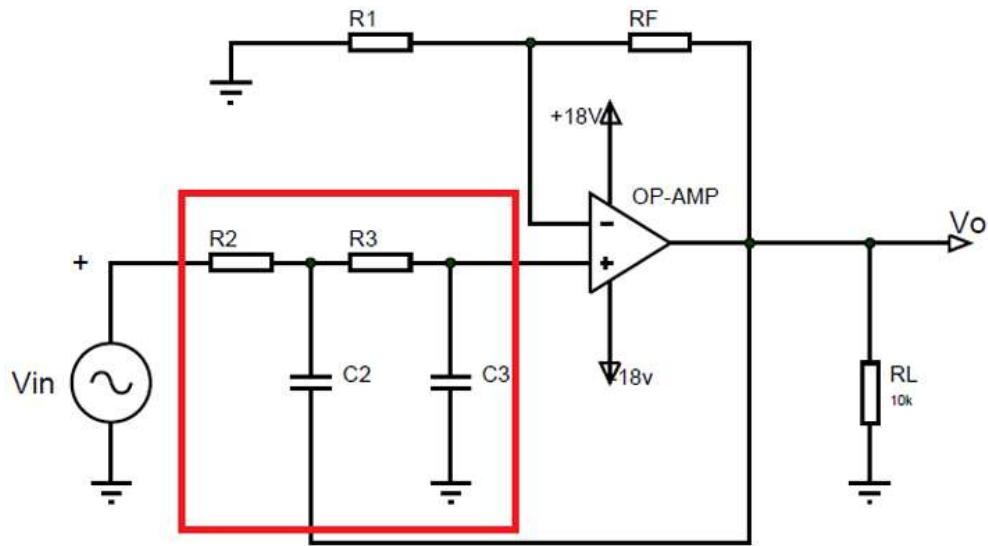$$\frac{v_{out}}{V_{in}} = \frac{A_F}{1 + j\frac{f}{f_H}}$$
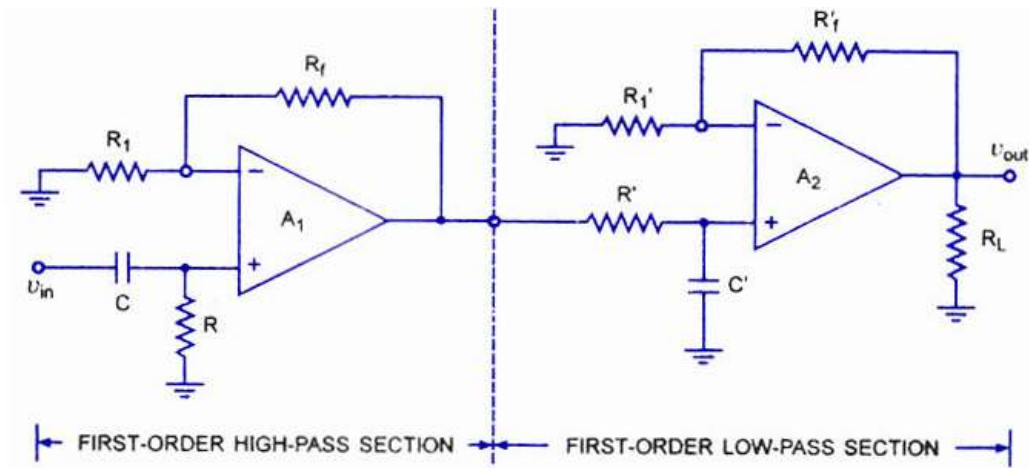
$$f_H = \frac{1}{2\pi RC}$$

b) Second order Low pass

$$\frac{V_O}{V_{in}} = A_F * \frac{\frac{1}{(R_2 C_2\, C_3 R_3)}}{S^2 + \frac{(R_2\, C_3 + R_2 C_2 + R_3 C_3 - R_2 C_2 A_F)S}{R_2 C_2\, C_3 R_3} + \frac{1}{(R_2 C_2\, C_3 R_3)}}$$

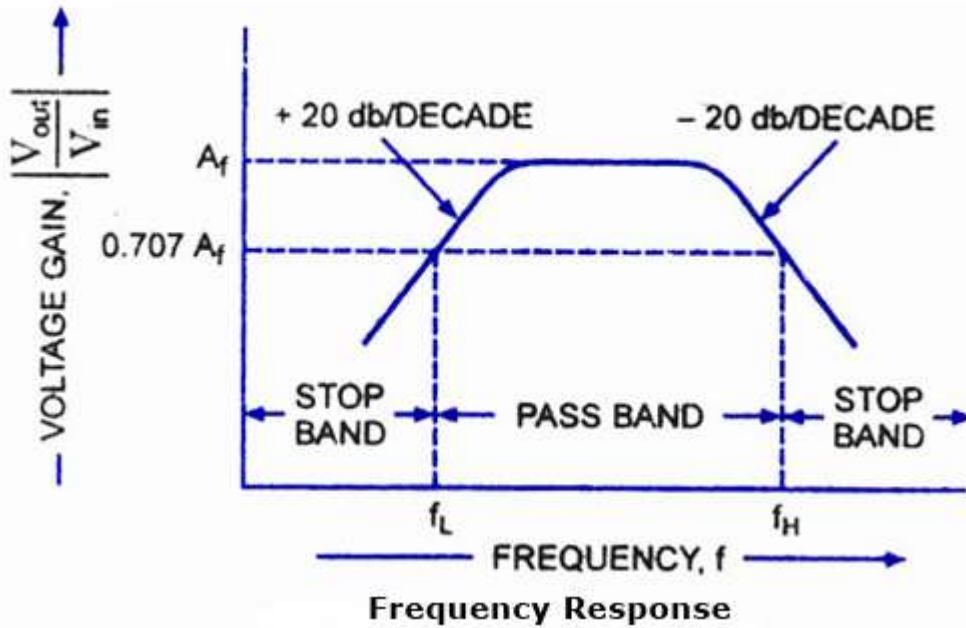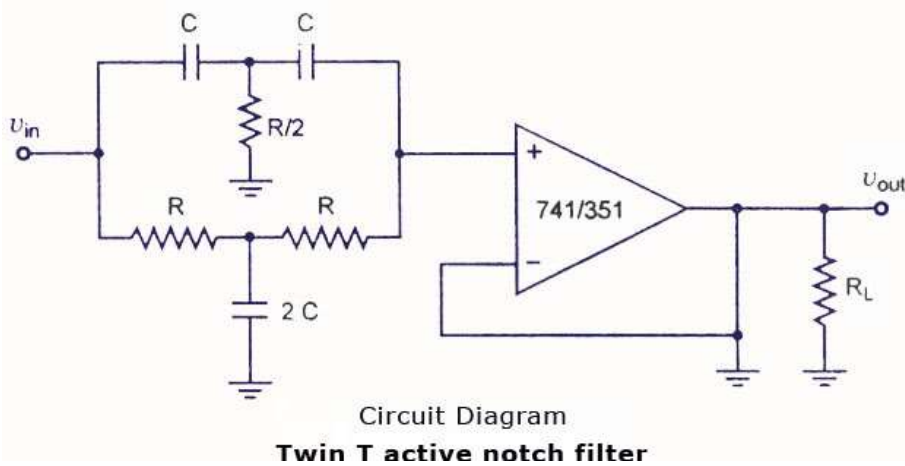$$f_H = \frac{1}{2\pi\sqrt{(R_2 C_2\, C_3 R_3)}}$$

c) Wide band pass filter

FIRST-ORDER HIGH-PASS SECTION | FIRST-ORDER LOW-PASS SECTION

$$\left|\frac{v_{out}}{V_{in}}\right| = \frac{A_{F2}A_{F1} * \frac{f}{f_L}}{\sqrt{\left\{1 + (\frac{f}{f_H})^2\right\}\left\{1 + (\frac{f}{f_L})^2\right\}}}$$
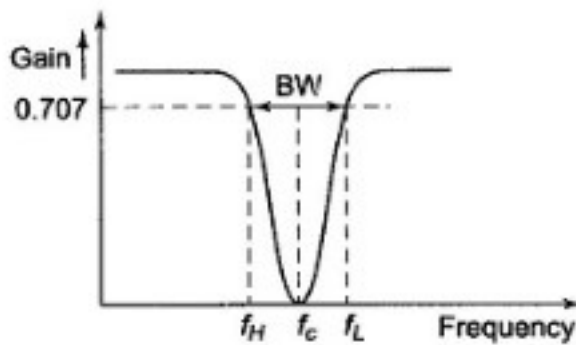
$$f_H = \frac{1}{2\pi R^1 C'}$$

$$f_L = \frac{1}{2\pi RC}$$

Frequency Response

d) Narrow band reject filter

Circuit Diagram
Twin T active notch filter

Gain, 0.707, BW, f_H f_c f_L Frequency

$$f_N = \frac{1}{2\pi RC}$$

3. What are the different turn on methods of SCR? Explain each of them in detail.

Turn-on methods

A thyristor can be turned on from non-conducting state to a conducting state in several ways :—

① Forward voltage triggering — When V_{AK} is increased with gate ckt open, I_a will have avalanche breakdown at break over voltage V_{BO}. At this voltage, thyristor changes from OFF to ON state.

② Thermal triggering (temperature) — The width of the depletion layer of a thyristor decreases on increasing the junction temperature. So when the V_{AK} is very near to V_{BO}, the device can be triggered by increasing its junction temperature.

③ Radiation triggering (Light triggering).   9

Thyristor is bombarded by energy particles such
as neutrons or photons. With the help of this
external energy, electron hole pairs are generated
which will increase the number of charge carriers,
causing instantaneous flow of current. For this to
happen, the device must have high value of
rate of change of voltage $\left(\frac{dV}{dt}\right)$.

④ $\frac{dV}{dt}$ triggering — When SCR is in forward
biased mode, J_2 will remain reverse biased. J_2
has the characteristics of a capacitor due to charges
existing across the junction. If the voltage impressed
across the device is V, the charge Q, and the
junction capacitance C_j, then

$$i_c = \frac{dQ}{dt} = \frac{d}{dt}(C_j V) = C_j \frac{dV}{dt} + V \frac{dC_j}{dt}$$

C_j is constant.

$$\therefore \quad i_c = C_j \frac{dV}{dt}$$

so if rate of change of voltage, $\frac{dV}{dt}$ is
large, the device may turn on.

⑤ Gate triggering — Most commonly used method
By applying a positive signal at the gate, SCR
can be triggered much before the break over voltage.

Three types of gate triggering pulses are 5
used :-

(a) **Dc gate triggering** — DC voltage of proper magnitude and polarity is applied between gate and cathode. Disadv → No isolation, more gate loss.

(b) **Ac gate triggering** — Most used in all ac applications. Provides proper isolation between power and control circuits. Phase angle control will provide proper firing angle.

(c) **Pulse gate triggering** — Most popular method.

A sequence of gate pulses are given to turn on an SCR. This is known as Carrier frequency gating. A transformer is used for isolation. There is no need of applying continuous signals, so gate losses are very much reduced.

4. Draw the circuit and frequency response of a second order low pass filter. Derive an expression for the cut off frequency.
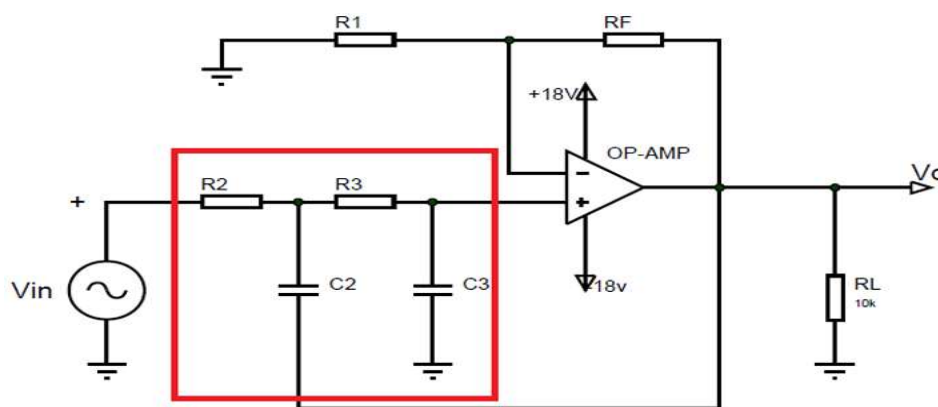
$jw = S$; capacitive reactance is $\dfrac{1}{SC}$
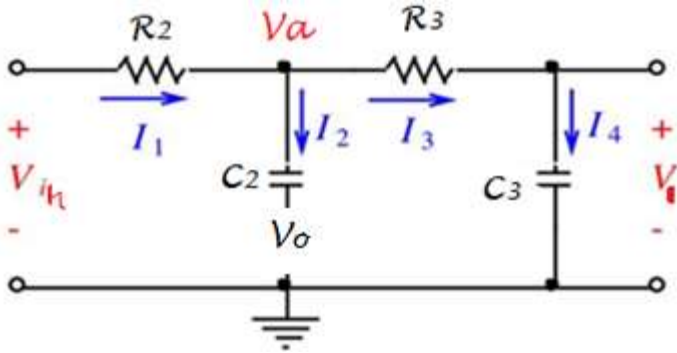
KCL Equations

$$V_{in} = (R_2 C_2\, C_3 R_3 S^2 + C_3 R_2 S + C_3 R_3 S + R_2 C_2 S - R_2 C_2 S A_F + 1)V_1$$

$$\frac{V_{in} - V_a}{R_2} = C_2 S(V_a - V_o) + \frac{V_a - V_1}{R_3}\frac{V_a - V_1}{R_3} = C_3 S V_1$$

$$V_a = (C_3 R_3 S + 1)V_1$$

$$V_{in} = (R_2 C_2 S + 1)V_a + R_2 * \frac{V_a - V_1}{R_3} - R_2 C_2 S V_o$$

$$V_{in} = (R_2 C_2 S + 1)V_a + R_2 * \frac{V_a - V_1}{R_3} - R_2 C_2 S V_o$$

$$V_{in} = (R_2 C_2 S + 1)V_a + R_2 * \frac{V_a - V_1}{R_3} - R_2 C_2 S V_o$$

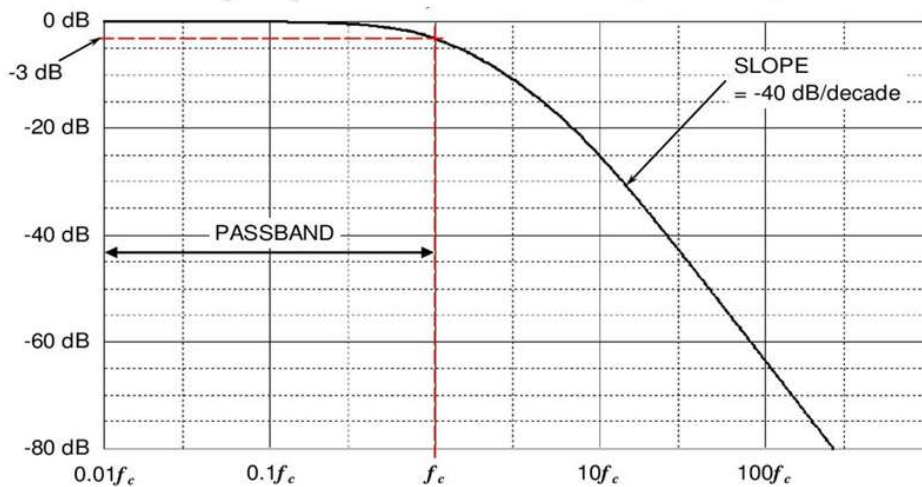$$V_{in} = (R_2 C_2 S + 1 + \frac{R_2}{R_3})V_a - V_1(\frac{R_2}{R_3} + R_2 C_2 S A_F)$$

$$V_{in} = (R_2 C_2 S + 1 + \frac{R_2}{R_3}) (R_3\, C_3 S + 1)V_1 - V_1(\frac{R_2}{R_3} + R_2 C_2 S A_F)$$

$$\frac{V_1}{V_{in}} = \frac{\frac{1}{(R_2 C_2 \, C_3 R_3)}}{S^2 + \frac{(R_2 \, C_3 + R_2 C_2 + R_3 C_3 - R_2 C_2 A_F)S}{R_2 C_2 \, C_3 R_3} + \frac{1}{(R_2 C_2 \, C_3 R_3)}}$$

$$\frac{V_O}{V_{in}} = A_F * \frac{\frac{1}{(R_2 C_2 \, C_3 R_3)}}{S^2 + \frac{(R_2 \, C_3 + R_2 C_2 + R_3 C_3 - R_2 C_2 A_F)S}{R_2 C_2 \, C_3 R_3} + \frac{1}{(R_2 C_2 \, C_3 R_3)}}$$

$$\omega_n = \frac{1}{\sqrt{(R_2 C_2 \, C_3 R_3)}} f_H = \frac{1}{2\pi \sqrt{(R_2 C_2 \, C_3 R_3)}}$$

$$\left| \frac{v_{out}}{V_{in}} \right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^4}}$$

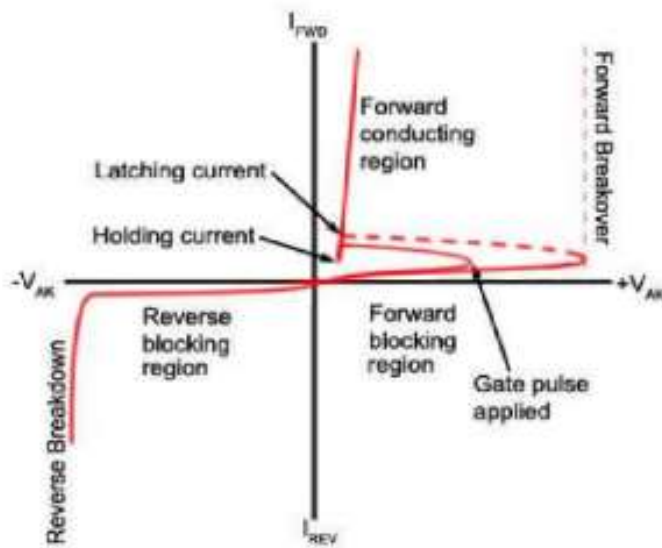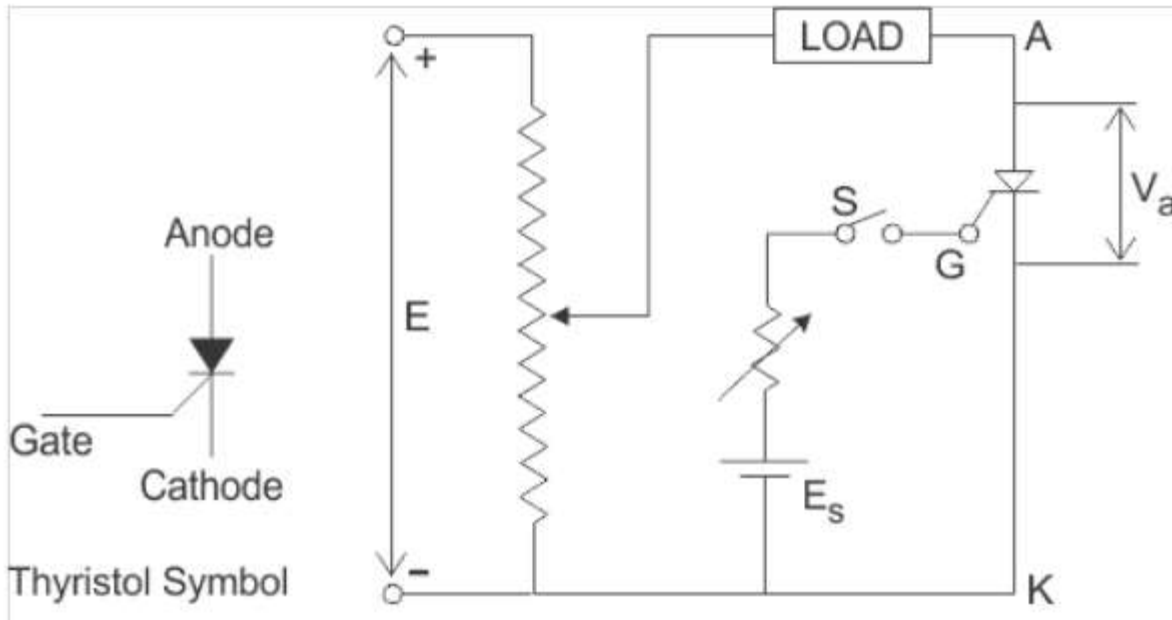$$\frac{V_O}{V_{in}} = A_F * \frac{\frac{1}{RC^2}}{S^2 + \frac{(3 - A_F)S}{RC} + \frac{1}{RC^2}}$$
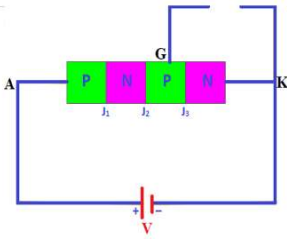
$$2\zeta = 3 - A_F$$

For Butter-worth Approximation

$\zeta = 0.707, then\ A_F = 1.586$

5. Explain the static Anode – Cathode characteristics of SCR with circuit diagram and VI characteristics. Define Latching and Holding Currents.

Circuit diagram

Forward Blocking mode

In this mode of operation, the positive voltage is applied to the anode and the negative voltage applied to the cathode, there will not be any pulse applied to the gate, it will be kept in the open state. Once the voltage is applied, the junctions J1 and J3 will be forward biased and the junction J2 will be reverse biased. Since J2 is reverse biased the width of the depletion region increases and it acts as an obstacle for conduction, so only a small amount of current will be flowing from J1 to J3.

Forward Conduction Mode
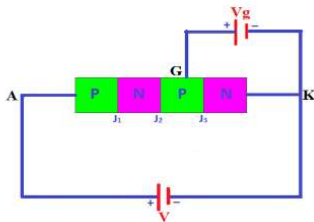
The Forward Conduction Mode is the only mode at which the SCR will be in the ON state and will be conducting. We can make the SCR conduct in two different ways, one we can increase the applied forward biasWhen we increase the Applied forward bias voltage between the anode and cathode the junction J2 will be depleted due to the avalanche breakdown and the SCR will start conducting. We are not able to do this for all the applications and this method of activating the SCR will eventually reduce the lifetime of the SCR.If you want to use the SCR for low voltage applications you can apply a positive voltage to the gate of the SCR. The applied positive voltage will help the SCR to move to the conduction state. During this mode of operation, the SCR will be operating in forward bias and current will be flowing through it. voltage beyond the breakdown voltage or else we can apply a positive voltage to the gate terminal.

Reverse Blocking Mode

In the reverse blocking mode, the positive voltage is applied to the Cathode (-) and the Negative voltage is given to the Anode (+), There will not be any pulse given to the gate, it will be kept as an open circuit. During this mode of operation the Junctions J1 and J3 will be reverse biased and the junction J2 will be forward biased. Since the junctions J1 and J3 are reverse biased there will not be any current flowing through the SCR. Although there will be a small leakage current flowing due to the drift charge carriers in the forward-biased Junction J2, it is not enough to turn on the SCR.
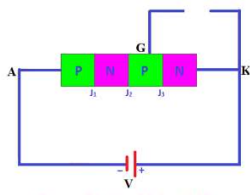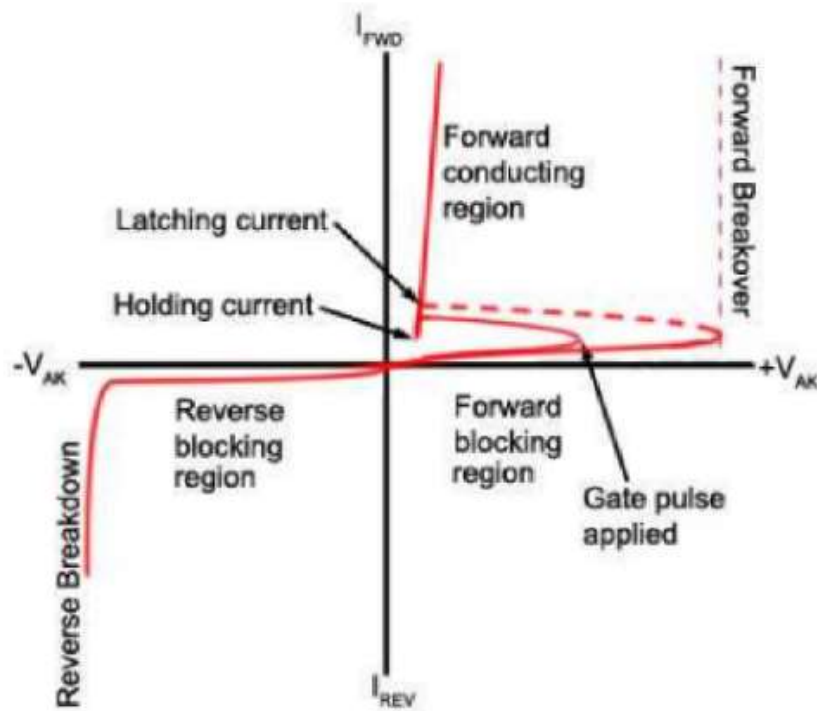
1. Breakover Voltage- It is the minimum forward voltage, gate being open, at which SCR starts conducting heavily i.e. turned on. Commercially available SCRs have breakover voltages from about 50 V to 500 V.

2. Peak Reverse Voltage (PRV)- It is the maximum reverse voltage (cathode positive w.r.t. anode) that can be applied to an SCR without conducting in the reverse direction.

Latching current of forward biased SCR is the minimum current which anode current must attain to continue to remain in forward conduction mode even when gate current is removed.

Holding current of SCR or thyrsistor is that minimum value of current below which anode current must fall to come in OFF state.

6. Explain the working of UJT and how UJT firing circuit is used for triggering an SCR.

The Unijunction Transistor or UJT for short, is a solid state three terminal device that can be used in gate pulse, timing circuits and trigger generator applications to switch and control either thyristors and triac's for AC power control type applications. Like diodes, unijunction transistors are constructed from separate P-type and N-type semiconductor materials forming a single (hence its name Uni-Junction) PN-junction within the main conducting N-type channel of the device.
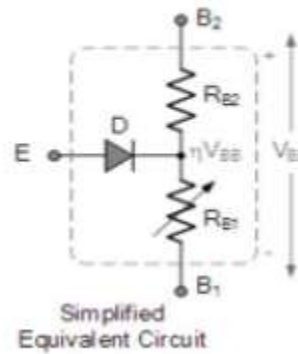
UJT Symbol — Construction — Simplified Equivalent Circuit
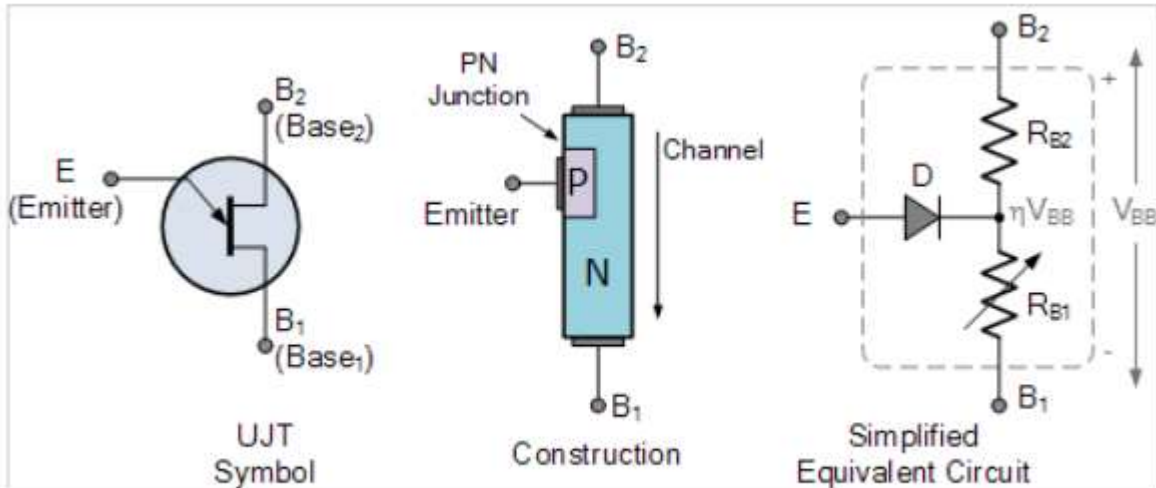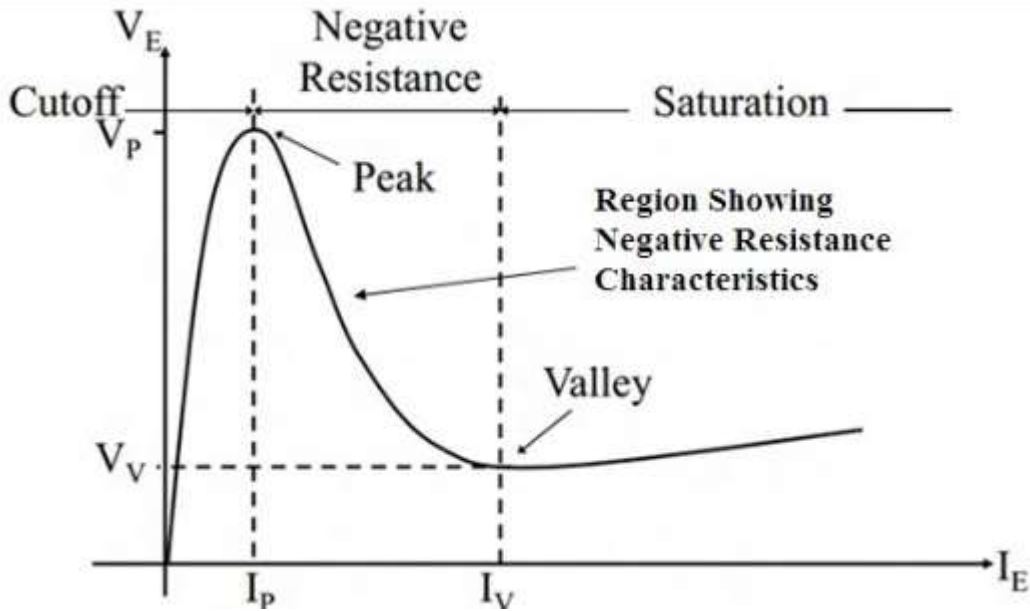
Unijunction Transistor (UJT)

- For a Unijunction transistor, the resistive ratio of R_{B1} to R_{BB} is called the **intrinsic stand-off ratio (η)**.

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

- Typical standard values of η range from 0.5 to 0.8 for most common UJT's.


Simplified Equivalent Circuit

Characteristics

 If a small positive input voltage which is less than the voltage developed across resistance, RB1 (ηVBB) is now applied to the Emitter input terminal, the diode p-n junction is reverse biased, thus offering a very high impedance and the device does not conduct. The UJT is switched "OFF" and zero current flows.

However, when the Emitter input voltage is increased and becomes greater than VRB1 (or ηVBB + 0.7V, where 0.7V equals the p-n junction diode volt drop) the p-n junction becomes forward biased and the unijunction transistor begins to conduct. The result is that Emitter current, ηIE now flows from the Emitter into the Base region.

The effect of the additional Emitter current flowing into the Base reduces the resistive portion of the channel between the Emitter junction and the B1 terminal. This reduction in the value of RB1 resistance to a very low value means that the Emitter junction becomes even more forward biased resulting in a larger current flow. The effect of this results in a negative resistance at the Emitter terminal.

UJT Firing Circuit
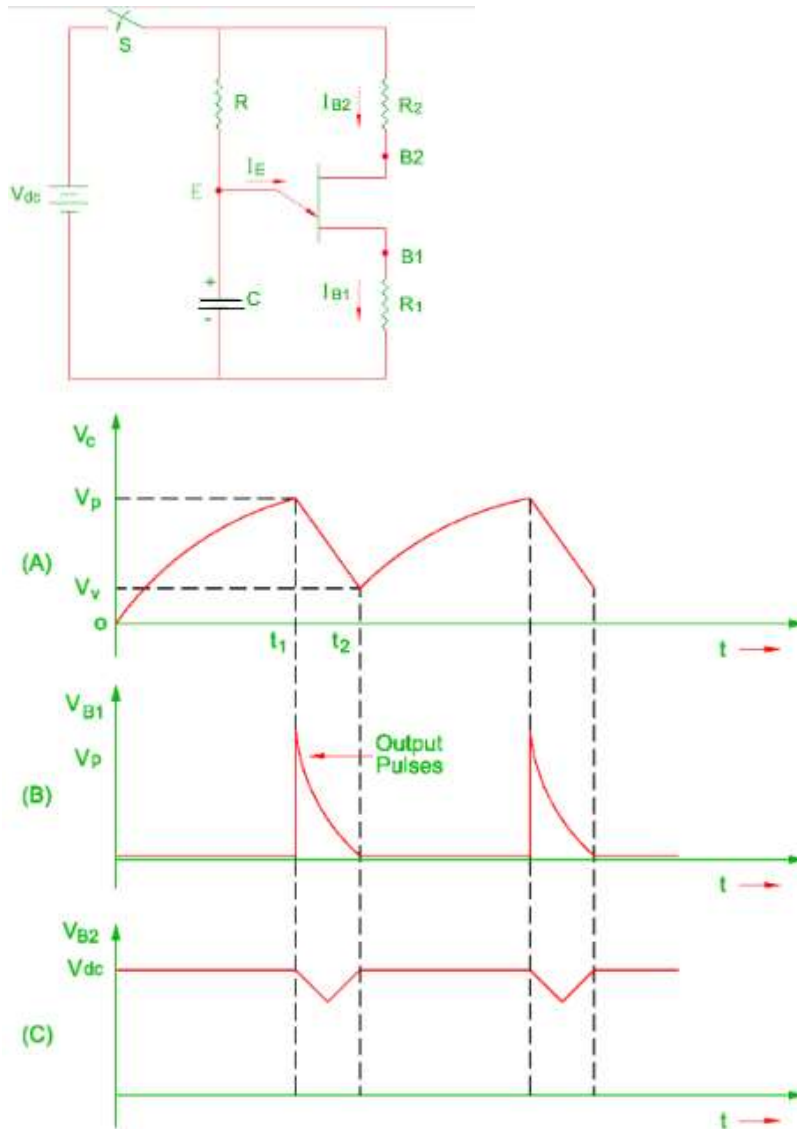
It is the most common method of triggering the SCR. The prolonged pulses at the gate using R and RC triggering methods cause more power dissipation at the gate. So by using UJT (Uni Junction Transistor) as triggering device the power loss is limited as it produce a train of pulses. The RC network is connected to the emitter terminal of the UJT which forms the timing circuit. The capacitor is fixed while the resistance is variable and hence the charging rate of the capacitor depends on the variable resistance means that the controlling of the RC time constant.

The UJT is often used in the timing and triggering circuits. Figure A shows the circuit diagram for the UJT relaxation oscillator. When the switch S is kept closed, the capacitor C is charged through resistance R towards voltage VDC. The voltage across capacitor in a given time depends upon circuit time constant RC.

When the voltage across capacitor becomes equal to peak point voltage, the emitter diode is forward biased and UJT conducts. As soon as the UJT starts to conduct, the capacitor discharges through inter base resistance RB1 and the resistance R1. The discharging time constant of the capacitor is very small as compared to charging time constant. The discharging time constant of the capacitor is very small as

compared to charging time constant. When the voltage across capacitor becomes less than the valley point voltage during discharging of the capacitor, the UJT comes in to non-conducting state. (It means that the UJT remains in conducting state until the emitter current drops below valley current).

The capacitor charging and discharging waveform is shown in the Figure A in which time t1 denotes for charging time and time t2 denotes for discharging time of the capacitor.

As the discharging time of the capacitor is very small as compared to charging time, the time required to complete one cycle is considered only for charging time of the capacitor.

$T = RC \, Log_e (Vdc / (Vdc – Vp))$

As $Vp = \eta Vdc + VD$

Where Vp = Peak point voltage

η = Intrinsic stand off ratio

VD = Threshold voltage of the diode

$T = RC \, Log_e (Vdc /(Vdc – \eta Vdc – VD))$

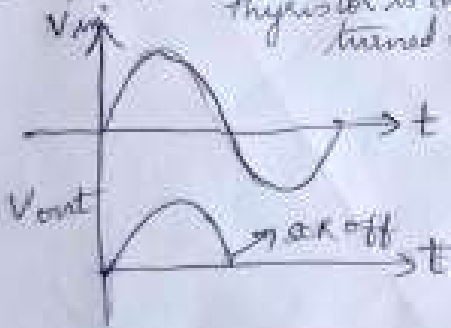As VD is small, it is neglected.

$T = RC \, Log_e (1 / (1 – \eta))$

7. What is commutation? What are the different types of Commutation? Explain class A commutation in detail.

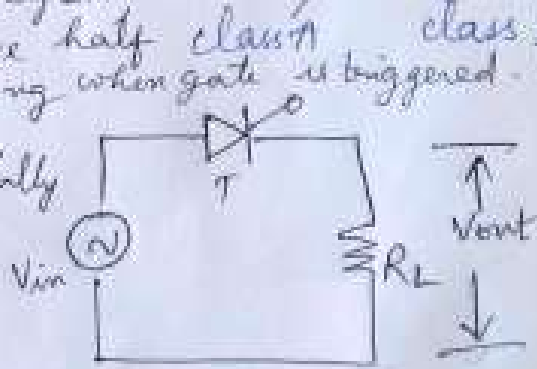The process of turning of SCR is called commutation.

Turn-off Methods

Natural Commutation   **Forced Commutation**

<u>Natural:-</u> As given in the ckt diagram
i/p signal will be ac during the half   **class A**   **class B**
cycle. thyristor will be conducting when gate is triggered. when
the i/p goes to negative half
thyristor is naturally
turned off.

Forced Commutation (class A)

This type of commutation uses L-C components in series with the load. We can have two combinations of class A circuit. ① when R_L in parallel with Capacitor ② when R_L is in series with C. Both the circuit forms an underdamped resonant circuit.
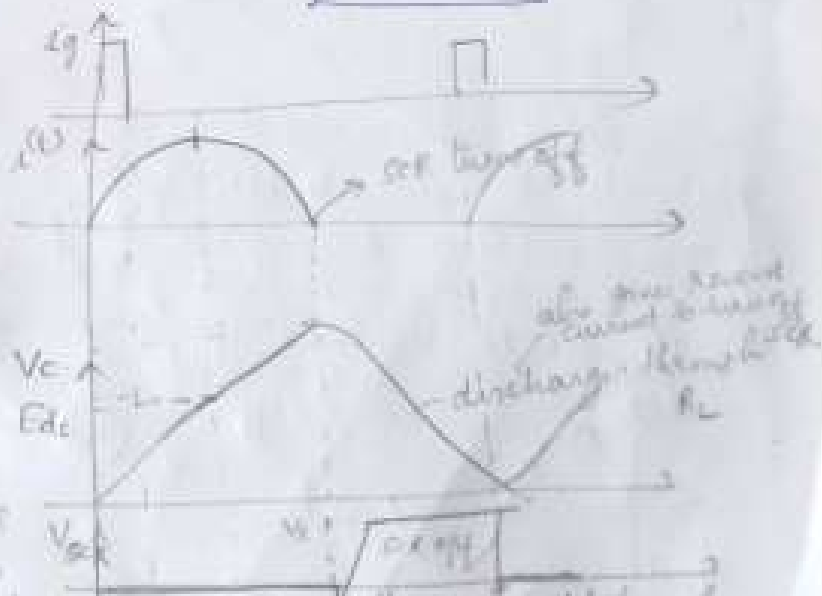
Capacitor charges gradually because
Presence of Inductor

when
$V_c = V_s$,
L changes
L polarity
and
C reverse
current starts flows
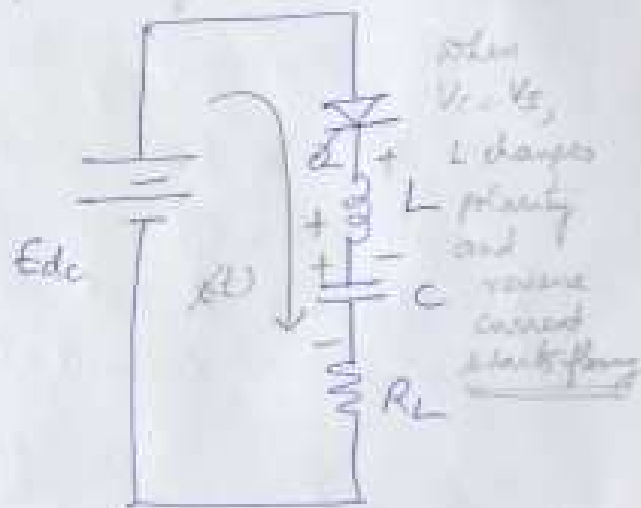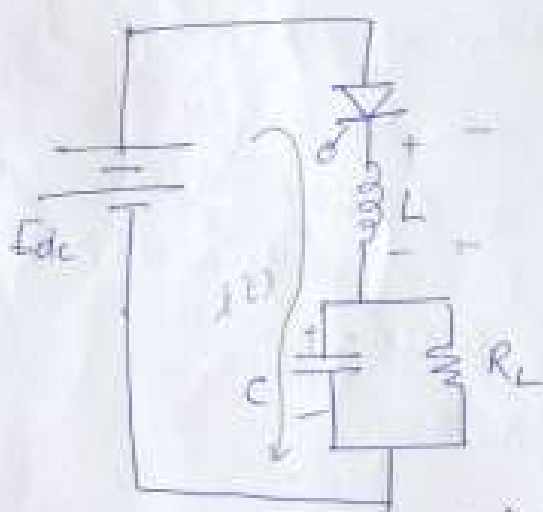
$C \rightarrow$ charges to Edc initially

During that time
i(t) increases gradually

when $V_c = Edc$
Inductor turns to change polarity. But it is having $V_t = Edc$ stored in it, which will give additional voltage to C so capacitor V_c increases.

But I opposes current flow.

car turns off

also the resonant current is having discharge through R_L

When an underdamped resonant circuit is excited by a dc source, the current will automatically become zero after some time. The thyristor when ON, carries only the charging current of capacitor C, and will soon reduce to a value lesser than the holding current of the SCR. This will switch off the thyristor (SCR). The time for switching off the device is determined by the resonant frequency which in turn depends upon the L and C components and the total load resistance.

8. With a neat circuit diagram, explain the working of a Resistance Firing circuit. Determine the trigger angle α for the following specifications:- Ig(min) = 0.1mA, Vg(min) = 0.5 V. The diode is silicon and the peak amplitude of the input is 24 volts. Rv = 100kΩ, Rmin = 10 kΩ.

Numerical Part:

Solution: The first step is to determine the instantaneous value of e_s at which triggering will occur. At the SCR trigger point, $V_{g(min)} = 0.5V$ and $I_{g(min)} = 0.1$ mA. Using KVL around the gate circuit, we have

$$e_s = I_g (R_V + R_{min}) + V_D + V_g$$

At the trigger point,

$e_{s(trigger)} = 0.1$ mA $(110 \text{ k}\Omega) + 0.7V + 0.5V = 12.2$ V.

Since e_s is a sine-wave, it obeys the expression

$$e_s = E_{max} \cdot \sin \omega t = E_{max} \cdot \sin(2\pi ft)$$

where $2\pi ft$ is the phase angle at any instant of time. For our purposes, this angle is α. Thus, $E_{max} = 24$ V,

$$e_s = 24 \sin \alpha. \qquad \therefore \quad 12.2 = 24 \sin \alpha.$$

$$\sin \alpha = \frac{12.2}{24} \qquad \therefore \quad \alpha = 30.6°.$$

<u>Resistance firing circuit</u> — The circuit in the figure shows a simple method of for varying the trigger angle and thereby the power to the load. Instead of using a gate pulse to trigger the SCR, gate current is supplied by an ac voltage source e_s, through R_{min}, R_V and diode D.
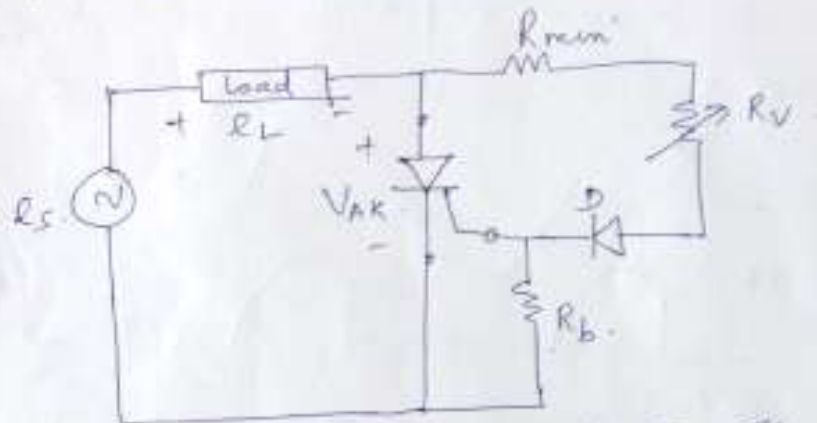

(i) As e_s goes positive, SCR is FB. It will not conduct until gate current exceeds $I_g min$ to trigger SCR.

(ii) e_s forward biases D, allowing gate current to start flowing.

(iii) When I_g reaches, $I_g min$ required to trigger SCR, SCR will then ON and e_L will be equal to e_s.

(iv) SCR remains ON till the +ve half cycle is over and the when e_s goes to zero, load current also reduces. When the load current goes below holding current, SCR turns off.

(v) SCR remains in the off state for the whole
-ve half cycle and will turn on only when
I_{gmin} triggers SCR again.

(vi) The purpose of diode is to prevent the gate-cathode
reverse bias from exceeding peak reverse voltage
during -ve half cycle of e_s.

(vii) The sequence is repeated.
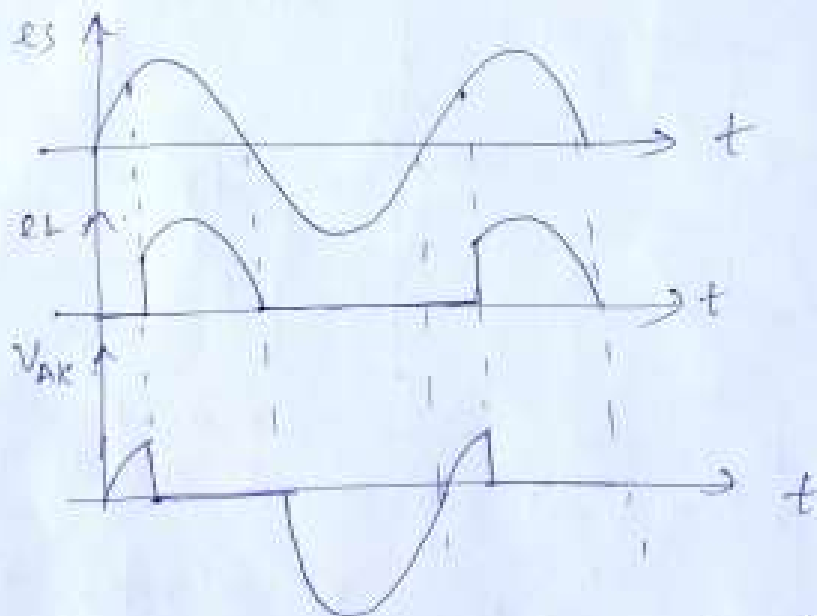
If R_v is increased, then gate current will reach
its trigger value I_{gmin} for a greater value of e_s,
making the SCR to turn off at a later stage.
The the firing angle α will increase.

R_{min} is required to ensure that the peak
gate current of the thyristor I_{gm} is not exceeded.

$$R_{min} \geq \frac{E_{max}}{I_{gm}}$$

R_b is a stabilising resistor so that the maximum voltage drop across it should not exceed max possible gate voltage V_{gmax}.

$$R_b \leq \frac{(R_v + R_{min})\, V_{gmax}}{e_{max} - V_{gmax}}$$

The thyristor will trigger when the instantaneous anode voltage e_s is

$$e_s = I_{gmin}\left(R_v + R_{min}\right) + V_d + V_{gmin}$$

- circuit is the simplest and most economical
- <u>Disadvs</u> ∝ is dependent on $I_{g\,min}$ which will vary from SCR to SCR and is temp dependent
- ∝ can be varied from 0 to 90° only
- e_s is max at its 90° point