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INTERNAL ASSESSMENT TEST – III

Sub	DIGITAL SIGNAL PROCESSING							Code	18EC52
Date	19/01/2023	Duration	90 mins	Max Marks	50	Sem	V	Branch	ECE

Answer any 5 full questions

		Marks	CO	RBT
1	With a neat block diagram, explain digital signal processors based on Harvard architecture. What are the differences between Harvard architecture and Von Neumann architecture?	[10]	CO5	L2
2a	Find the signed Q-15 representation of -0.560123	[05]	CO5	L2
2b	Find the floating point representation of -0.638454×2^5. Use 4 bits to represent exponent and 8 bits for mantissa.	[05]	CO5	L2
3a	Explain IEEE single precision format and IEEE double precision format.	[06]	CO5	L2
3b	Convert the following IEEE single precision format number into decimal format. $110000000.0100 \ldots 00$	[04]	CO5	L2

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Page 1 of 2

		Marks	CO	RBT
4	Explain the following DSP hardware units. i) Multiplier and Accumulator (MAC) ii) Shifter iii) Address Generator	[10]	CO5	L2
5	Design an FIR filter for the following desired frequency response using rectangular window. $H_d(\omega) = \begin{cases} 0 & for\ \lvert\omega\rvert < \frac{\pi}{4} \\ e^{-j4\omega} & for \frac{\pi}{4} \le \lvert\omega\rvert \le \pi \end{cases}$	[10]	CO4	L3
6	Derive an expression for the transfer function and the frequency response of TYPE-I (Odd, Symmetric) and TYPE-II (Even, Symmetric) FIR filters.	[10]	CO4	L3
7	Draw the direct form-I and direct form-II realizations of the filter whose difference equation is given by $y[n] - 0.5y[n-1] + 0.75y[n-2] = 2x[n] - 3x[n-1]$ Also, obtain the transfer function of the filter.	[10]	CO4	L3
8	Obtain the cascade form realization of the system whose transfer function is $H(z) = \frac{(z-0.5)(z-0.25)}{(z-0.4)(z-0.6)}$	[10]	CO4	L3

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Page 2 of 2

Scheme Of Evaluation

Internal Assessment Test III – Jan 2023

Sub:	DIGITAL SIGNAL PROCESSING							Code:	18EC52
Date:	19/ 01 / 2023	Duration:	90 mins	Max Marks:	50	Sem:	V	Branch:	ECE

Note: Answer All Questions

Question #		Description	Marks Distribution		Max Marks
1		With a neat block diagram, explain digital signal processors based on Von Neumann architecture. What are the differences between Harvard architecture and Von Neumann architecture?		10	10
		• Block diagram • Explanation • Differences	2 6 2		
2a		Find the signed Q-15 representation of -0.560123		05	10
		• Q-15 representation • 2s complement	3 2		
2b		Find the floating point representation of -0.638454×2^5. Use 4 bits to represent exponent and 8 bits for mantissa.		05	
		• Mantissa • Exponent	3 2		
3a		Explain IEEE single precision format and IEEE double precision format.		06	10
		• Single Precision • Double Precision	3 3		
3b		Convert the following IEEE single precision format number into decimal format. 110000000.0100 ... 00		04	10
		• Decimal	04		
4		Explain the following DSP hardware units. i) Multiplier and Accumulator (MAC) ii) Shifter iii) Address Generator		10	10
		• MAC • Shifter • Address Generator	2 2 6		
5		Design an FIR filter for the following desired frequency response using Hanning window. $H_d(\omega) = \begin{cases} 0 & for\ \lvert\omega\rvert < \frac{\pi}{4} \\ e^{-j4\omega} & for\ \frac{\pi}{4} \le \lvert\omega\rvert \le \pi \end{cases}$		10	10

		• Impulse Response • Window Equation • Product	6 2 2		
6		Derive an expression for the transfer function and the frequency response of TYPE-III (Odd, Antisymmetric) and TYPE-IV (Even, Antisymmetric)FIR filters.		10	10
		• Type 1 • Type 2	5 5		
7		Draw the direct form-I and direct form-II realizations of the filter whose difference equation is given by $y[n] - 0.5y[n-1] + 0.75y[n-2] = 2x[n] - 3x[n-1]$ Also, obtain the transfer function of the filter.		10	10
		• DF-I • DF-II • Transfer function	4 4 2		
8		Obtain the cascade form realization of the system whose transfer function is $H(z) = \frac{(z-0.5)(z-0.25)}{(z-0.4)(z-0.6)}$		10	10
		• System 1 • System 2 • Cascade	4 4 2		

1. Architecture of Microprocessors

Microprocessor architecture can be classified as

- Von Neumann Architecture
- Harvard Architecture

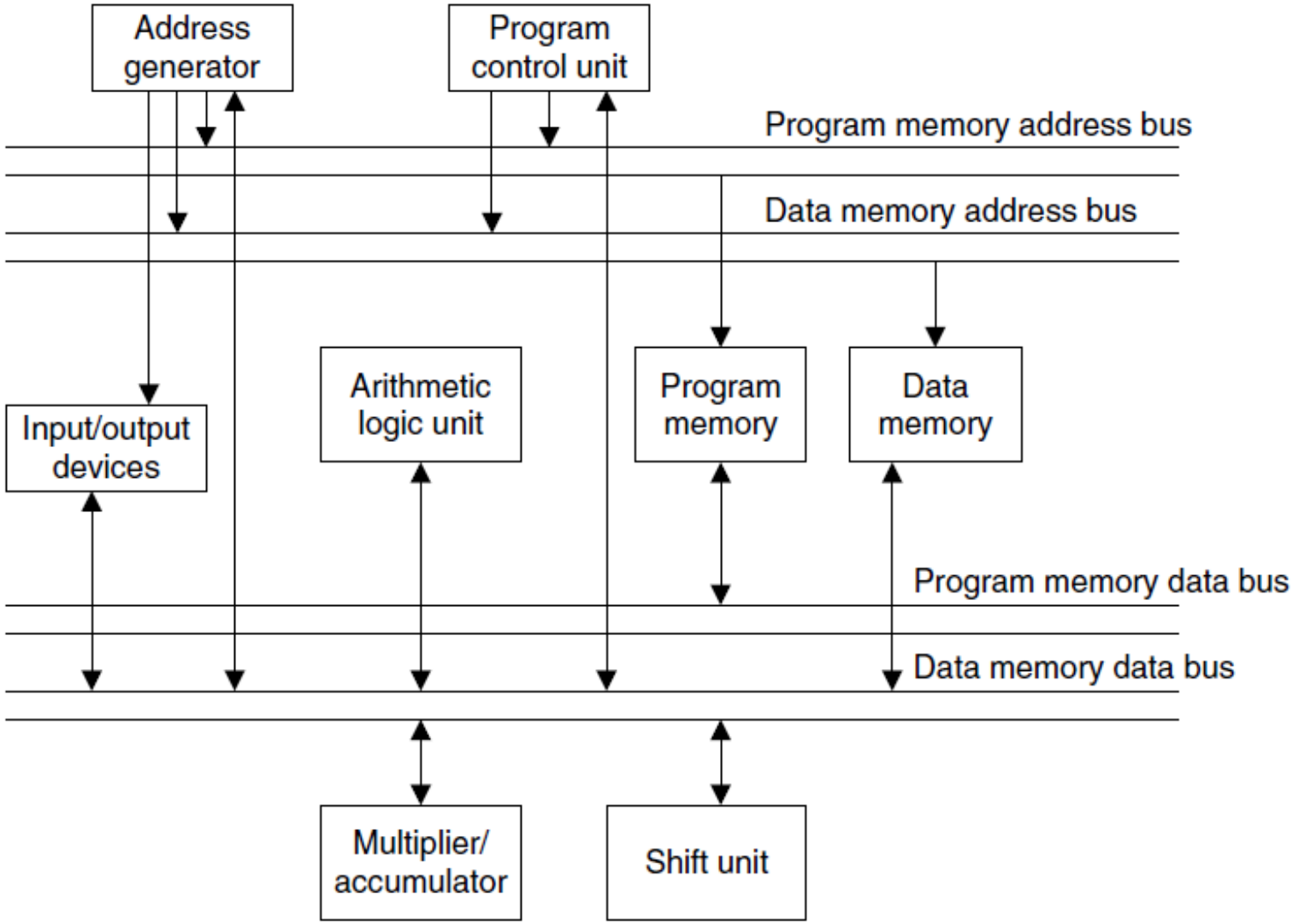
The design of general purpose microprocessors and microcontrollers is based on the Von Neumann architecture.

Digital Signal Processors (DSPs) are designed with Harvard Architecture.

Harvard Architecture

The main components of a processor designed with Von Neumann Architecture are

- Arithmetic Logic Unit
- Program Control Unit
- Address Generator
- Program Memory
- Data Memory


Address generator
Program control unit
Program memory address bus
Data memory address bus
Input/output devices
Arithmetic logic unit
Program memory
Data memory
Program memory data bus
Data memory data bus
Multiplier/ accumulator
Shift unit

- Harvard architecture has two separate memory units - one is dedicated to the program code, while the other is dedicated for data.
- To accommodate two memory spaces, two corresponding address buses and two data buses are used.
- This means that the Harvard processor can fetch the program instruction and data in parallel at the same time.
- There is an additional unit called a multiplier and accumulator (MAC), which is dedicated for the digital filtering operation.
- The last additional unit, the shift unit, is used for the scaling operation for fixed-point implementation when the processor performs digital filtering.

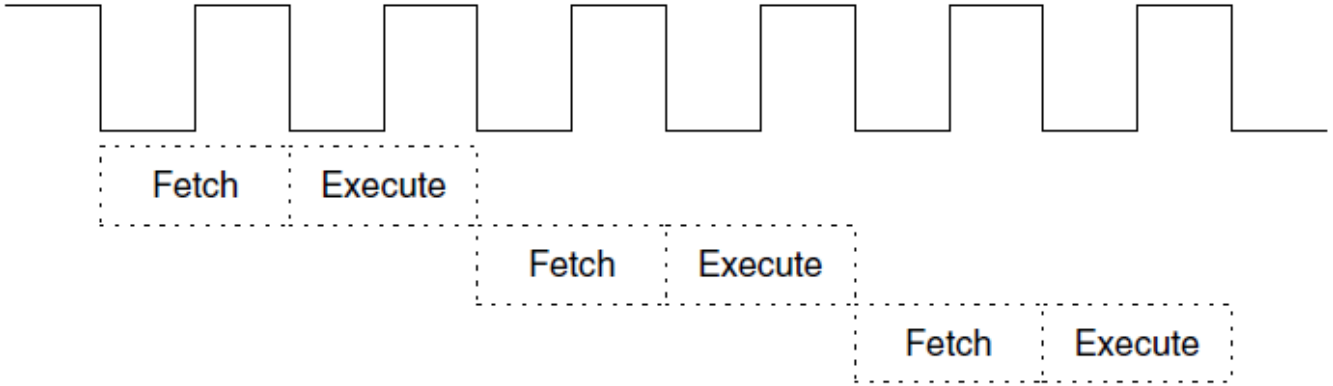


Fig. 3. Execution cycle based on Von Neumann architecture

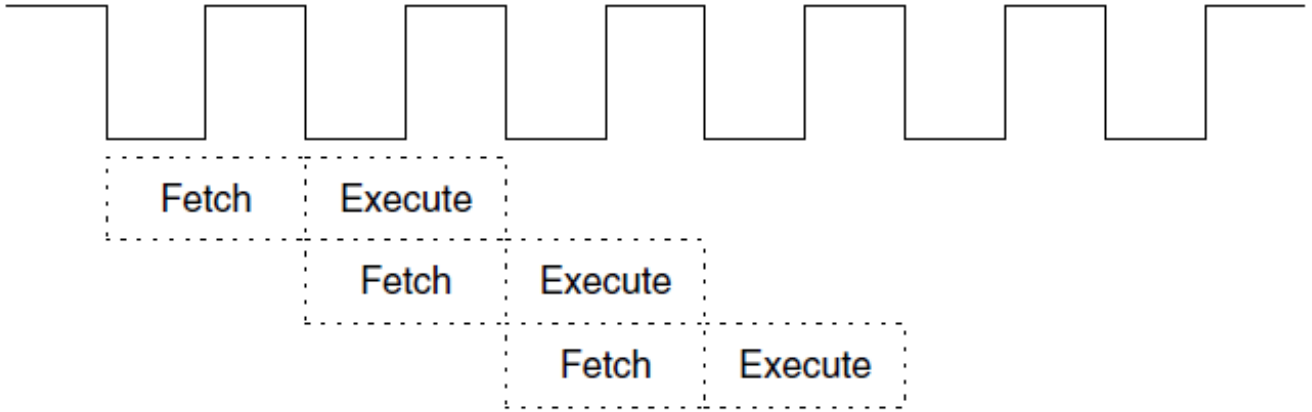


Fig. 4. Execution cycle based on Harvard architecture

- Fig. 3 shows the execution cycle based on Von Neumann architecture.
- Instruction fetch and execute cycles take place in serial fashion.
- Fig. 4 shows the execution cycle based on Harvard architecture.
- While the current instruction is being executed, the next instruction to be executed is fetched.
- This is called pipelining.
- Pipelining dramatically increases the processing speed.

The Harvard architecture is preferred for all digital signal processors due to the requirements of most DSP algorithms, such as filtering, convolution, and FFT, which need repetitive arithmetic operations, including multiplications, additions, memory access, and heavy data flow through the CPU

For other applications, such as those dependent on simple microcontrollers with less of a timing requirement, the Von Neumann architecture may be a better choice, since it offers much less silica area and is thus less expansive.

2. Find the signed Q-15 representation of 0.560123.

Number	Product	Carry
0.560123×2	1.120246	1 (MSB)
0.120246×2	0.240492	0
0.240492×2	0.480984	0
0.480984×2	0.961968	0
0.961968×2	1.923936	1
0.923936×2	1.847872	1
0.847872×2	1.695744	1
0.695744×2	1.391488	1
0.391488×2	0.782976	0
0.782976×2	1.565952	1
0.565952×2	1.131904	1
0.131904×2	0.263808	0
0.263808×2	0.527616	0
0.527616×2	1.055232	1
0.055232×2	0.110464	0 (LSB)

MSB, most-significant bit; LSB, least-significant bit.

Table 3 : Conversion process of 0.560123 into Q-15 format

Hence,

$$0.560123 = 0.10001110110010$$

Note that first bit is 0 because the number is +ve.

4. Digital Signal Processor (DSP) Hardware Units

Some of the special units in a DSP are

- Multiplier and Accumulator (MAC)
- Shifter
- Address Generator

Multiplier and Accumulator (MAC)

- MAC is a special hardware unit for enhancing the speed of digital filtering.
- Fig. 5 shows a typical MAC unit used in DSP.
- It has a pair of input registers, each holding a 16-bit input to the multiplier.
- The result of the multiplication is accumulated in a 32-bit accumulator unit.
- The result register holds the double precision data from the accumulator.

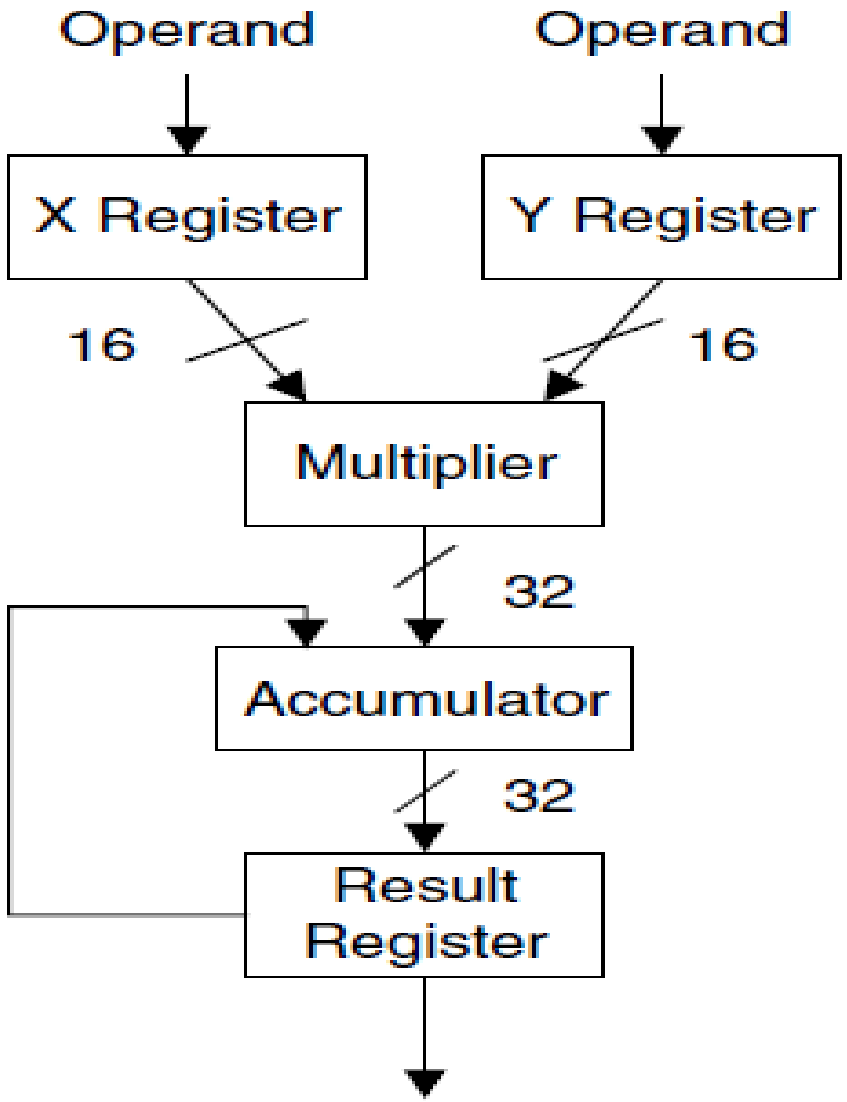


Fig. 5. The multiplier and accumulator (MAC) dedicated to DSP

Shifter

- Consider a 3-bit data word.

$$(011)_2 = (3)_{10}$$

- Shifting $(011)_2$ to the right gives $(001)_2 = (1)_{10}$
- It is as good as dividing 3 by 2 and then truncating the fractional part.
- Consider a 3-bit data word.

$$(011)_2 = (3)_{10}$$

- Shifting $(011)_2$ to the left gives $(110)_2 = (6)_{10}$
- It is as good as multiplying 3 by 2.
- A DSP requires these operations to be done quite often.
- Hence, it uses a special hardware unit for shifting.

Address Generators

- In a DSP, data samples are stored in a circular buffer.
- Figure 6 describes the basic mechanism of circular buffering for a buffer having eight data samples.

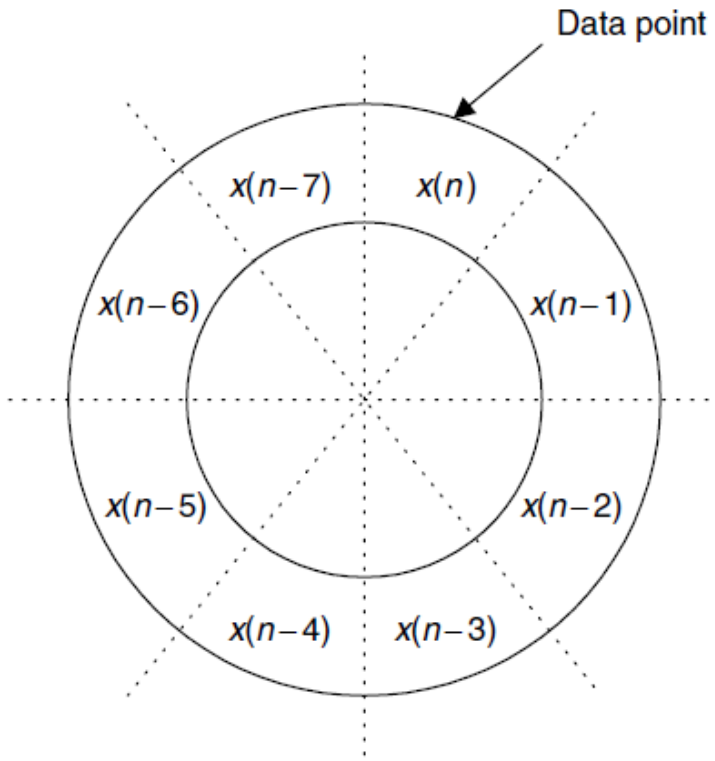


Fig. 6. Illustration of circular buffering

- In circular buffering, a pointer is used and it always points to the newest data sample.
- After the next sample is obtained from analog to digital converter (ADC), the data will be placed at the location of $x(n-7)$ and the oldest sample is pushed out.
- Thus, the location for $x(n-7)$ becomes the location for the current sample.
- The original location for $x(n)$ becomes the location of the past sample $x(n-1)$.
- For each new data sample, only one location on the circular buffer needs to be updated.

- The circular buffer acts like a first-in/first-out (FIFO) buffer, but every data sample on the buffer need not be moved.
- This will significantly enhance the processing speed.
- Fig. 7 gives a simple illustration of 2-bit circular buffer.

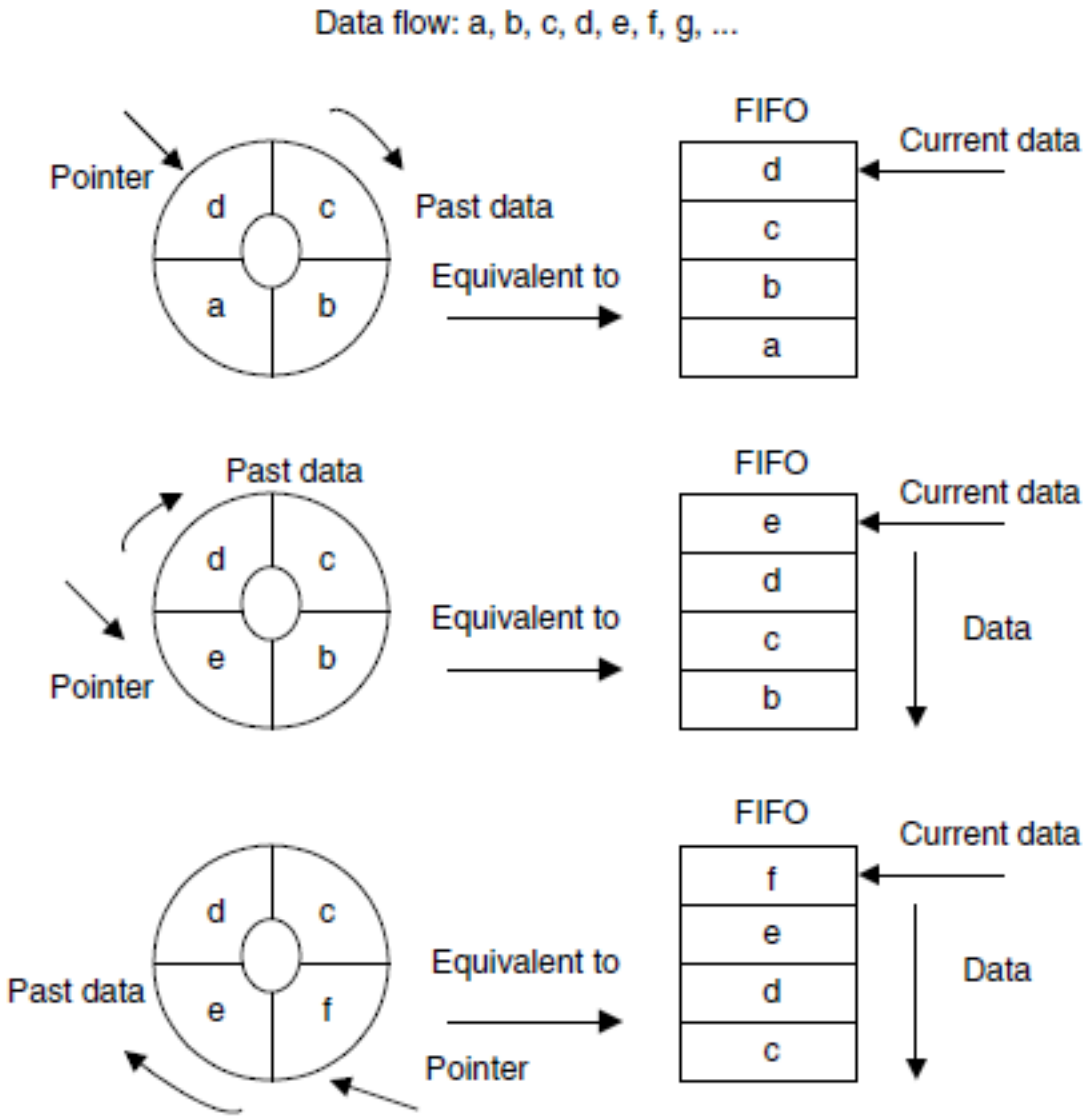


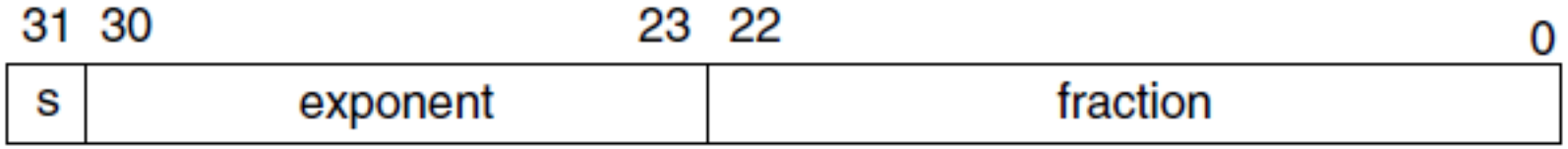
Fig. 7. Circular Buffer and Equivalent FIFO Operation

- Initially, the buffer is storing the samples a,b,c,d and the pointer is pointing to (storing the address of) the latest sample d.
- The equivalent FIFO buffer is shown on the right.
- When the new sample e comes in, it will be stored in the place of the oldest sample i.e., a and pointer now points to the position of e.
- Note that only one position in the circular buffer is updated.
- But, if the same operation is to be implemented with the help of FIFO buffer, all the 4 locations are to be updated.

3. IEEE Floating Point Formats

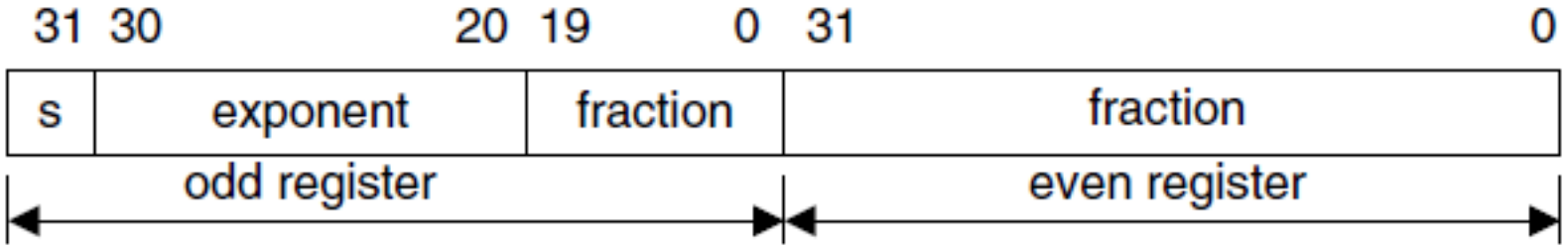
- IEEE stands for Institute of Electrical and Electronics Engineers
- It was formed in 1963 with the objectives of the educational and technical advancement of electrical and electronic engineering, telecommunications, computer engineering and allied disciplines
- There are two types of IEEE floating-point formats
- One is the IEEE single precision format, and the other is the IEEE double precision format.

IEEE Single Precision Format (IEEE 754)



$$x = (-1)^S \times (1.F) \times 2^{E-127}$$

IEEE Double Precision Format (IEEE 754)



$$x = (-1)^s \times (1.F) \times 2^{E-1023}$$

IAT-3 Solutions

2a) Q-15 representation of -0.560123

$0.100011111011\,0010$

$1.011100001001\,101$

$\qquad\qquad\qquad\qquad\quad 1$

$1.011100001001\,110$ (2's compl)

2b) Floating point representation of -0.638454×2^5

4 bits - exponent
8-bits - mantissa

0.1010001

1.0101110

$\qquad\quad\;\; 1$

1.0101111

$0101\;\;10101111$

exp mantissa

3a) Single Precision

32 bits
1 sign bit
8 exp bits
23 fraction bits

$d = (-1)^S (1.F)(2^{E-127})$

Double Precision

64 bits
1 sign bit
11 exp bits
52 fraction bits

$d = (-1)^S (1.F)(2^{E-1023})$

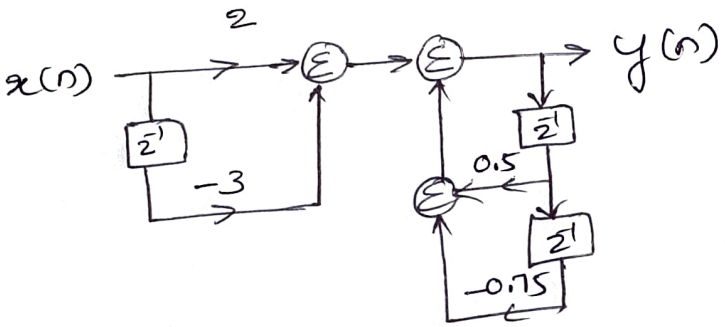
3b) $11000000000.010\ldots00$

$d = (-1)^{S=1} (1.25)(2^{128-127}) = -1.25 \times 2 = -2.5$

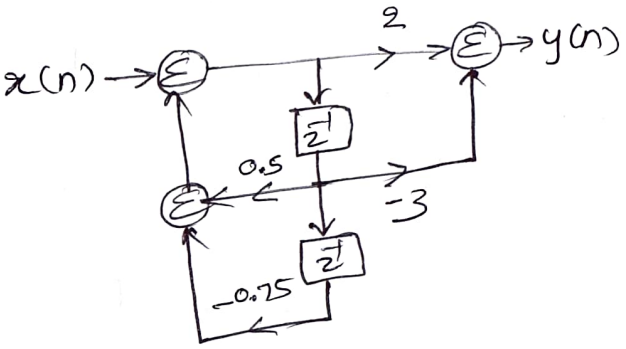
5) $$h(n)=\begin{cases}\dfrac{-\sin\left(\frac{\pi}{4}(n-4)\right)}{\pi(n-4)}, & n\neq 4\\ 0.75=\dfrac{3}{4}, & n=4\end{cases}$$

$$h(n)=(0,\ -0.075,\ -0.1592,\ -0.2251,\ 0.75,\ \ldots)$$

6) $$H(z)=\frac{2-3z^{-1}}{1-0.5z^{-1}+0.75z^{-2}}$$



DF-I



DF-II

8) $$H(z)=\frac{(z-0.5)(z-0.25)}{(z+0.4)(z-0.6)}=\frac{(1-0.5z^{-1})(1-0.25z^{-1})}{(1+0.4z^{-1})(1-0.6z^{-1})}$$