CBCS SCHEME

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21EE42

Fourth Semester B.E. Degree Examination, June/July 2023
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Design a circuit to cube a 2-bit number. Implement using minimum number of only NAND gates. **(07 Marks)**

b. Explain Maxterm canonical form with an example. Express the given Boolean function in proper canonical form with decimal notation.

$f(w,x,y,z) = (\bar{w}+x)(y+\bar{z})$. **(06 Marks)**

c. Convert the given Boolean expression into :
i) Minterm canonical form

ii) Maxterm canonical form $f(p,q,r) = P(\bar{q}+\bar{r})$. **(07 Marks)**

OR

2 a. Simplify the following function using Quine -Mc Cluskey technique.
$f(a, b, c, d) = \Sigma m(0, 4, 5, 9) + \Sigma dc(1, 7, 13)$.
Also obtain the minimal SOP form using Karnaugh map and verify the result. **(12 Marks)**

b. List all the prime implicants of the given function and obtain the minimal SOP form using Karnaugh Map.
$Y(a, b, c, d) = \Sigma m(0, 1, 2, 3, 4, 7, 8, 9) + \Sigma dc(10, 11, 12, 13, 14, 15)$. **(08 Marks)**

Module-2

3 a. Design a combinational logic circuit that will convert BCD digit to Excess-3 BCD digit using gates. Construct a truth table and simplify each output equation using Karnaugh maps. **(08 Marks)**

b. Implement the following function pairs using 74138IC and gates with minimum number of inputs.
$f_1(a, b, c) = \Sigma m(0, 2, 4)$ $f_2(a, b, c) = \Sigma m(1, 2, 4, 5, 7)$. **(06 Marks)**

c. Implement a 1-bit comparator using a decoder. **(06 Marks)**

OR

4 a. Implement the function : $f(a, b, c, d) = \Sigma m(1, 1, 5, 6, 7, 9, 10, 15)$ using a 4 : 1 Mulitplexer with a, b as select inputs. **(08 Marks)**

b. Implement a 4-bit carry look Ahead adder and explain how carry propagation delay is eliminated in a carry look ahead adder. **(12 Marks)**

Module-3

5 a. Explain how the switch bounce effect is eliminated by the use of an SR latch with the help of timing diagram. **(08 Marks)**

b. Explain the working of a Master-solve JK flip-flop with timing diagram. **(12 Marks)**

OR

6 a. Obtain the characteristic equations for T, D SR and JK flip-flop. **(10 Marks)**

b. Explain the working of a Master Slave SR flip-flop with timing diagram. **(10 Marks)**

Module-4

7 a. Explain the working of a universal shift Register with neat circuit diagram. **(09 Marks)**

b. Explain the operation of a 4-bit binary ripple counter using –ve edge triggered JK flip-flops giving the timing diagram. **(06 Marks)**

c. Draw the circuit diagram and timing diagram for MOD-12 ripple UP-counter using T flip-flops. **(05 Marks)**

OR

8 a. Design a MOD-8 twisted Ring counter using positive edge triggered D flip-flops and give the count sequence and timing diagram. **(08 Marks)**

b. Design a synchronous counter using positive edge triggered JK flip-flops for the count sequence 0, 1, 4, 6, 7, 5 ...... **(12 Marks)**

Module-5

9 a. Explain Mealy and Moore models in sequential circuits with block diagrams and examples. **(08 Marks)**

b. Design a synchronous circuit using positive edge triggered JK flip-flops to generate the flowing sequence :

$0 \rightarrow 1 \rightarrow 2 \rightarrow 0$ if Input X = 0 and

$0 \rightarrow 2 \rightarrow 1 \rightarrow 0$ if Input X = 1

Provide an output which becomes equal to '1' to indicate non-zero present state when X = 0. **(12 Marks)**

OR

10 a. Analyze the following sequential circuit and obtain :

i) Flip-flop input and output equations
ii) Transition table
iii) State table
iv) State diagram.

(Refer Fig.Q10(a)).

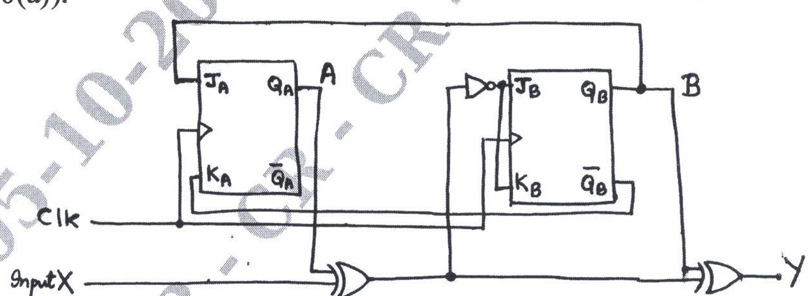

Fig.Q10(a) **(12 Marks)**

b. Write short notes on :

i) Read only memory
ii) Programmable ROM
iii) EPROM
iv) Flash memory. **(08 Marks)**

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