CBCS SCHEME

USN

21EE32

Third Semester B.E. Degree Examination, June/July 2023
Analog Electronic Circuits and Op-Amps

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. For the clipper circuit shown in Fig.Q.1(a), draw the output voltage waveform and transfer characteristics. **(07 Marks)**

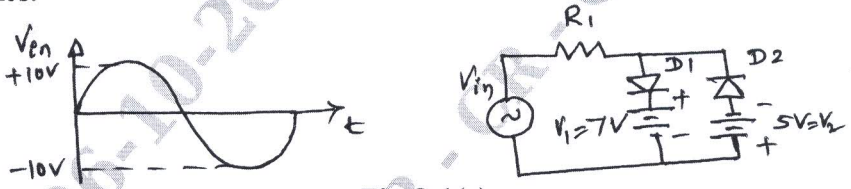

Fig.Q.1(a)

b. Find the operating point for the voltage divider bias circuit with $\beta = 80$ and $V_{BE} = 0.6V$. Find the new operating point when β changes to 100 and V_{BE} changes to 0.25. Given: $V_{CC} = 15V$, $R_1 = 100K\Omega$, $R_2 = 18K\Omega$, $R_C = 10K\Omega$, $R_E = 1K\Omega$. **(07 Marks)**

c. With neat circuit and waveforms, explain the operation of positive clamper. **(06 Marks)**

OR

2 a. For the circuit shown in Fig.Q.2(a), find the operating point for $R_B = 150K\Omega$ and $R_B = 300K\Omega$. **(08 Marks)**

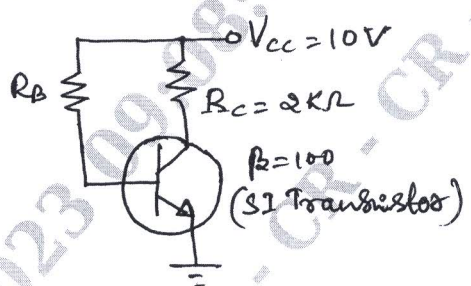

Fig.Q.2(a)

b. Define and explain h-parameters. **(05 Marks)**

c. With neat circuit and waveforms, explain the common Emitter amplifier limit. **(07 Marks)**

Module-2

3 a. Explain the need of cascading amplifier. Draw and explain the block diagram of n-stage cascaded amplifier. **(07 Marks)**

b. An amplifier with open loop voltage gain of 1000 delivers 10W of power output at 10% second harmonic distortion when the input is 10mV. If 40dB negative feedback is applied and power output remaining 10W. Determine required input signal V_S and second harmonic distortion with feed back. **(06 Marks)**

c. Derive an expressions for Z_i, A_i and A_v for Darlington Emitter follower. **(07 Marks)**

OR

4 a. Derive an expression for gain of a feedback amplifier with negative feedback. **(06 Marks)**

b. If an amplifier has bandwidth of 300kHz and voltage gain of 100. What will be the new bandwidth and gain if 10% negative feedback is introduced? What will be the gain bandwidth product before and after feedback? What should be the amount of feedback if the bandwidth is to be limited to 800kHz? **(07 Marks)**

c. Draw the neat diagram of voltage series feedback amplifier and also derive expression for input resistance. **(07 Marks)**

Module-3

5 a. How classification of power amplifier is done based on the location of Q-point? Also indicate the operating cycle in each case. **(08 Marks)**

b. Explain the operation of push pull class B power amplifier. Also show that the maximum efficiency is 78.5%. **(07 Marks)**

c. For a class-A amplifier with V_{CC} = 20V driving an 8Ω load, determine:

i) DC power

ii) Maximum output power

iii) Maximum limit efficiency. **(05 Marks)**

OR

6 a. Explain the construction, working and characteristics of n-channel JFET. **(10 Marks)**

b. Explain the construction, working and characteristics of depletion type MOSFET. **(10 Marks)**

Module-4

7 a. Explain with a neat diagram inverting and non-inverting summing amplifiers. **(10 Marks)**

b. What is an instrumentation amplifier? Obtain an expression for input voltage V_0, in terms of change in resistance ΔR of an instrumentation amplifier using transducer bridge. **(10 Marks)**

OR

8 a. With a neat limit diagram explain working of 1st order low pass filter and its typical frequency response curve. **(10 Marks)**

b. An LM317 regulator is to provide 6V output from 15V supply. The load current is 200mA. Determine the suitable resistance values for R_1 and R_2, and calculate the regulator power dissipation. **(04 Marks)**

c. Mention the advantages of active filter over passive filter (any six). **(06 Marks)**

Module-5

9 a. With a neat limit diagram, explain the working of triangular/rectangular wave generator. **(10 Marks)**

b. Design a RC phase shift oscillator using Op-amp for a frequency of 500 Hz. Also draw the limit diagram and name the component values take C = 0.1MF. **(06 Marks)**

c. With a neat limit diagram, explain comparator as a zero crossing detector. **(04 Marks)**

OR

10 a. With a neat limit diagram and necessary derivation for load current, explain voltage to current converter with grounded load. **(10 Marks)**

b. With a neat limit diagram, explain inverting comparator as Schmitt trigger. **(10 Marks)**

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