CBCS SCHEME

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17EE34

Third Semester B.E. Degree Examination, June/July 2023
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain diode positive shunt clipper circuit with I/O waveforms and transfer characteristics. **(06 Marks)**

b. With neat diagram and waveforms explain the working of a negative clamper. **(06 Marks)**

c. For the clipper circuit shown in the Fig.Q.1(c), the input is $V_i = 50 \sin wt$. Plot the o/p voltage waveform and transfer characteristics. **(08 Marks)**

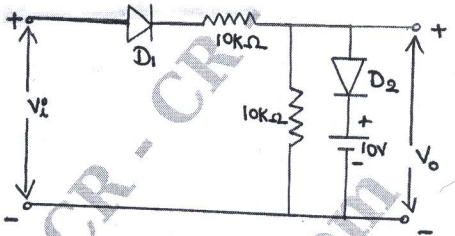

Fig.Q.1(c)

OR

2 a. Explain emitter bias circuit, with the help of base-emitter and collector-emitter loop. Write the necessary equations. **(08 Marks)**

b. For the fixed bias circuit, derive expressions for S_{ICO}, S_β and S_{VBE}. **(06 Marks)**

c. An emitter bias configuration has the following specifications:

$I_{CQ} = \frac{1}{2} I_C\,(sat)$, $I_C\,(sat) = 8mA$, $V_{CC} = 18V$ and $\beta = 110$. Determine R_B, R_C and R_E. **(06 Marks)**

Module-2

3 a. Obtain the expressions for voltage gain, input and output impedance for Emitter bias circuit with unbypassed R_E using re model. **(10 Marks)**

b. For the network shown in Fig.Q.3(b), determine i) Z_i ii) Z_o iii) A_v iv) A_i. **(10 Marks)**

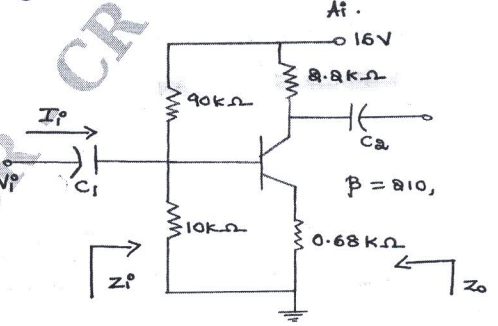

Fig.Q.3(b)

OR

4 a. Derive an expression for Z_i, Z_o, A_v and A_I for voltage divider bias configuration using approximate hybrid model. **(10 Marks)**

b. A transistor in CE mode has h-parameters; $h_{ie} = 1100\Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 100$, $h_{oe} = 25\mu A/v$. Determine the equivalent CB parameters. **(04 Marks)**

c. A voltage divider bias circuit has $R_1 = 47K\Omega$, $R_2 = 10K\Omega$, $R_C = 2.2K\Omega$, $R_E = 560\Omega$, $V_{CC} = 14V$. Assuming R_E is bypassed, determine voltage gain, i/p and o/p impedance. Take h-parameters of the transistor to be $h_{ie} = 1100\Omega$, $h_{fe} = 100$, $h_{oe} = 25\mu A/v$. **(06 Marks)**

Module-3

5 a. For the cascaded arrangement shown below in Fig.Q.5(a) determine:

i) The loaded gain for each stage.
ii) The total gain for the system A_v and A_{vs}
iii) The total current gain for the system
iv) The total gain for the system if the emitter follower configuration were removed.
v) The phase relation between v_o and v_i. **(10 Marks)**

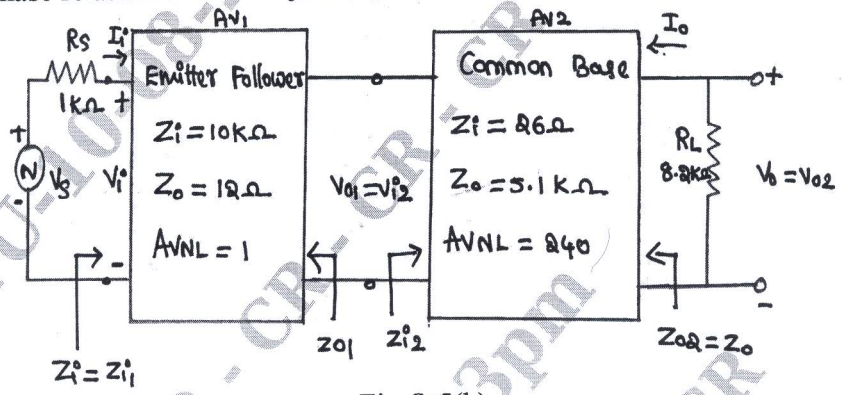

Fig.Q.5(b)

b. Derive expression for Z_i and A_I for a Darlington, Emitter follower circuit. **(10 Marks)**

OR

6 a. With the help of block diagram, explain the concept of feedback. **(08 Marks)**

b. For a current series feedback amplifier, derive an expression for output impedance with feedback. **(06 Marks)**

c. Determine the voltage gain, input and output resistance with feedback for voltage series feedback having A = -100, $R_i = 10K\Omega$, $R_0 = 20K\Omega$ for feedback of i) $\beta = -0.1$ ii) $\beta = -0.5$ **(06 Marks)**

Module-4

7 a. With neat circuit and waveforms, explain the operation of a transformer coupled class A power amplifier. **(10 Marks)**

b. Show that maximum efficiency of class = B push pull power amplifier circuit is 78.5%. **(10 Marks)**

OR

8 a. With a neat circuit diagram and waveform, explain the operation of RC phase shift oscillator using BJT. Write the expression for frequency of oscillation. **(10 Marks)**

b. With a neat circuit diagram and waveform, explain the working principle of crystal oscillator operating in series resonant mode. A crystal has L= 0.334H, C = 0.065pF and R = 5.5KΩ. Calculate its series resonant frequency. **(10 Marks)**

Module-5

9 a. List out the differences between BJT and FET. **(05 Marks)**

b. With the help of neat diagrams, explain the construction, working and characteristics of n-channel JFET. **(10 Marks)**

c. Obtain the expression for transconductance 'g_m' of JFET. **(05 Marks)**

OR

10 a. With a neat sketch, explain the construction and working principle of N-channel enhancement type MOSFET and also explain its static drain characteristics. **(10 Marks)**

b. Determine Z_I, Z_o and A_V for JFET common source amplifier with fixed bias configuration using AC equivalent small signal model. **(10 Marks)**

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