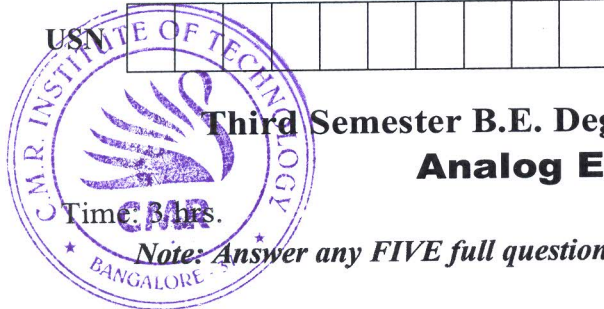


CBCS SCHEME

18EE34



Third Semester B.E. Degree Examination, June/July 2023 Analog Electronic Circuit

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Define Q or Operating point (02 Marks)
- b. What is a clipper circuit? Explain the working of a double ended clipper with a suitable diagram. (08 Marks)
- c. List various types of clamper circuit. With a neat circuit diagram, explain the working of a negative clamper. (10 Marks)

OR

- 2 a. Discuss emitter stabilized bias circuit. Also derive expression for I_B , I_C , V_B and V_C . (10 Marks)
- b. Determine the following for the fixed bias configuration of Fig.2(b). Assume $\beta=50$.
(i) I_{BQ} and I_{CQ} (ii) V_{CEQ} (iii) V_B and V_C (iv) V_{BC}

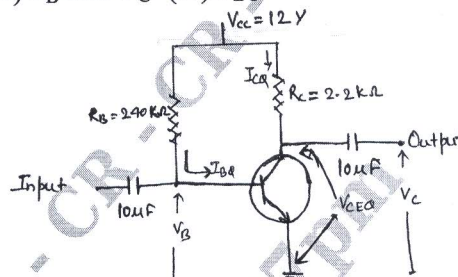


Fig.Q.2(b)

(10 Marks)

Module-2

- 3 a. Derive an expression for A_v , Z_i and Z_o of CE voltage divider bias circuit using hybrid model. (10 Marks)
- b. For the collector feedback configuration of Fig 3(b), calculate (i) r_e (ii) Z_i and Z_o (iii) A_v and A_f Consider $\beta=200$, $r_o=60K\Omega$.

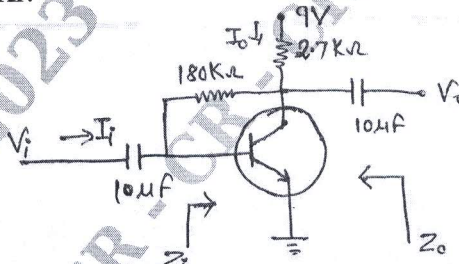


Fig.3(b)

(10 Marks)

OR

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

- 4 a. For the network of fig 4(a), determine: (i) r_e (ii) Z_i (iii) Z_o ($r_o = \infty$) (iv) A_v ($r_o = \infty$) (10 Marks)

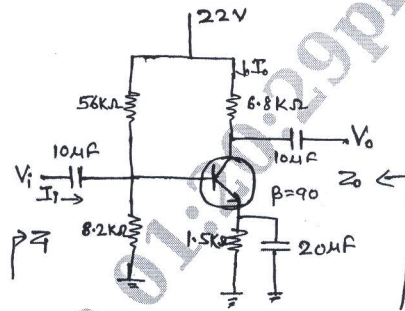


Fig.4(a)

- b. Why hybrid model is called as hybrid? Obtain h – parameters from equivalent circuit of common – emitter configuration. (10 Marks)

Module-3

- 5 a. Define Multistage Amplifier. Derive voltage gain and current gain of a two stage cascaded amplifier. (10 Marks)
- b. Derive an expression for Z_i and A_i for Darlington Emitter follower circuit. (10 Marks)

OR

- 6 a. Find out input and output impedance of a current series feedback amplifier. (10 Marks)
- b. Determine the voltage gain, input and output impedance with feedback for voltage series feedback having $A = -100$, $R_i = 10\text{ k}\Omega$, $R_o = 20\text{ k}\Omega$ for feedback of
i) $\beta = -0.1$ and ii) $\beta = -0.5$. (10 Marks)

Module-4

- 7 a. With a neat circuit diagram, explain the AC Operation of series – fed class – A amplifier. Also derive maximum efficiency of the amplifier. (10 Marks)
- b. Show that maximum efficiency of Class – B push pull power amplifier is 78.54%. (10 Marks)

OR

- 8 a. Explain the working of R.C phase shift oscillator. If $R = 1\text{ k}\Omega$, $R_c = 1\text{ k}\Omega$ and $C = 0.1\mu\text{f}$, Calculate the frequency of oscillations. (10 Marks)
- b. Discuss the working of Wein Bridge Oscillator, with a suitable diagram. (10 Marks)

Module-5

- 9 a. Describe the working and characteristics of M – Channel JFET. (10 Marks)
- b. For a self – bias circuit, $V_{DD} = +20$, $R_D = 3.3\text{ k}\Omega$, $R_G = 1\text{ M}\Omega$, $R_S = 1\text{ k}\Omega$, $I_{DSS} = 8\text{ mA}$ and $V_P = -6\text{ V}$. Determine i) V_{GS} ii) I_D iii) V_{DS} iv) V_S v) V_G vi) V_D . (10 Marks)

OR

- 10 a. With a neat structure, explain the operation of an n – channel depletion type MOSFET. (10 Marks)
- b. Compare JFET with MOSFET. Sketch the transfer characteristics for an N – channel depletion type MOSFET with $I_{DSS} = 10\text{ mA}$ and $V_P = -4\text{ V}$. (10 Marks)
