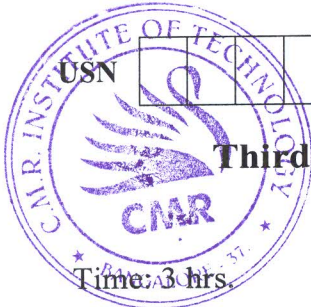


CBCS SCHEME

18EE35



Third Semester B.E. Degree Examination, June/July 2023 Digital System Design

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Simplify the following in SOP form using K-Map
 $f(A, B, C, D) = \overline{A} \overline{B} C + AD + \overline{B} D + \overline{C} D + A \overline{C}$ (05 Marks)
- b. Identify all prime implicants and essential prime implicants of the following functions using K-map $f(a, b, c, d) = \pi M(0, 2, 3, 8, 9, 10, 12, 14)$. (05 Marks)
- c. Using Quine McCluskey tabulation method, obtain the set of prime implicants for the function : $f(a, b, c, d) = \Sigma(0, 1, 4, 5, 9, 10, 12, 14, 15) + \Sigma\phi(2, 8, 13)$ and hence obtain the minimal form of the given function employing decimal representation. (10 Marks)

OR

- 2 a. Reduce the function using K-map technique :
 $F(A, B, C, D, E) = \Sigma m(1, 4, 8, 10, 11, 20, 22, 24, 25, 26) + d(0, 12, 16, 17)$. (10 Marks)
- b. Simplify using Quine McCluskey tabulation algorithm :
 $V = f(a, b, c, d) = \Sigma(2, 3, 4, 5, 13, 15) + \Sigma d(8, 9, 10, 11)$. (10 Marks)

Module-2

- 3 a. Explain the concept of carry look ahead adder. (07 Marks)
- b. Design and implement a 2 bit compactor. (08 Marks)
- c. Implement the following Boolean function with 8 : 1 multiplexer
 $F(A, B, C, D) = \Sigma m(0, 2, 6, 10, 11, 12, 13) + d(3, 8, 14)$. (05 Marks)

OR

- 4 a. Design a 4-bit parallel adder/subtractor using 7483. (10 Marks)
- b. Write the condensed truth table for a 4 to 2 line priority encoder with a valid output where the highest priority is given to the highest bit Position or input with highest index and obtain the minimal sum expressions for the outputs. (10 Marks)

Module-3

- 5 a. Explain the working of a master-slave JK FF with the help of logic diagram, function table, logic symbol and timing diagram. (10 Marks)
- b. Obtain the characteristic equation for D and T flip-flop. (06 Marks)
- c. What do you mean by sequential circuit? Explain the help of block diagram. (04 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 6 a. With a neat logic diagram, explain the working of positive edge triggered D flip-flop. (10 Marks)
 b. Explain race around condition. How is it eliminated? (05 Marks)
 c. Realize SR flip-flop using only NOR Gates. (05 Marks)

Module-4

- 7 a. Design BCD ripple counter using JK flip-flop. (10 Marks)
 b. Explain with suitable logic and timing diagram : (10 Marks)
 i) SISO
 ii) PIPO.

OR

- 8 a. Design a MOD-5 synchronous counter using JK flip-flop and implement it. Also draw the timing diagram. (10 Marks)
 b. Explain Johnson counter with its circuit diagram and timing diagram. (10 Marks)

Module-5

- 9 a. Explain Mealy model and Moore model for clocked synchronous sequential network. (10 Marks)
 b. A sequential circuit with 2D ffs A and B and input X and output Y is specified by the following next state and output equations :
 $A(t + 1) = AX + BX$
 $B(t + 1) = A' X$
 $Y = (A + B)X'$
 i) Draw the logic diagram of the circuit
 ii) Derive the state table
 iii) Derive state diagram. (10 Marks)

OR

- 10 a. A sequential circuit has one input and one output. The state diagram is shown in Fig.Q10(a). Design the sequential circuit with T flip-flop.

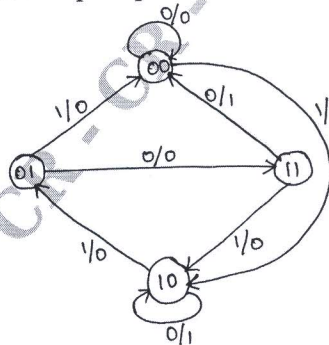


Fig.Q10(a)

- b. Write short notes on :
 i) PROM
 ii) Flash memory. (10 Marks)

CMRIT LIBRARY
 BANGALORE - 560 037
