CBCS SCHEME

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18EC56

Fifth Semester B.E. Degree Examination, June/July 2023
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain typical design flow for designing VLSI IC circuits with a neat flow chart. **(10 Marks)**

b. Explain top-down design methodology and bottom-up design methodology. **(06 Marks)**

c. Explain trends in HDL's. **(04 Marks)**

OR

2 a. Explain design hierarchy by taking 4-bit ripple carry counter. **(08 Marks)**

b. Define the following terms with examples "
i) Module
ii) Instances
iii) Instance name. **(06 Marks)**

c. Explain the different levels of abstraction used for programming in verilog. **(06 Marks)**

Module-2

3 a. With a neat block diagram, explain the components of verilog module. **(08 Marks)**

b. Explain $display, $monitor, $finish and $stop system tasks with examples. **(08 Marks)**

c. How to write comments in verilog HDL, explain with examples. **(04 Marks)**

OR

4 a. Explain the following data types of with an examples :
i) Nets
ii) Registers
iii) Integers
iv) Parameters. **(08 Marks)**

b. Write verilog description of SR latch. Also write stimulus code. **(08 Marks)**

c. With an example, explain hierarchical names. **(04 Marks)**

Module-3

5 a. What are Rise, Fall and Turn-off delays? How they are specified in verilog. **(06 Marks)**

b. Write a verilog dataflow level of abstraction for 4 to 1 multiplexer using conditional operator. Also write stimulus code. **(08 Marks)**

c. Design a gate level module according to the logic diagram given Fig.Q5(c). Write stimulus code delay.

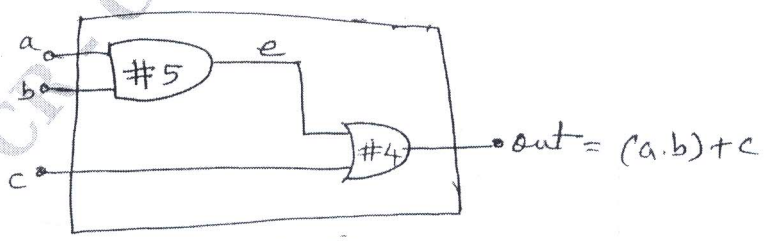

Fig.Q5(c) **(06 Marks)**

OR

6 a. Develop a gate-level verilog code for 4-bit ripple carry adder from 1-bit full adder. What is the output if A = 1010, B = 1100 and $c_{in} = 0$ at t = 0. **(10 Marks)**

b. What would be the output of the following :
a = 4'b0111, b = 4'b1001
i) &b
ii) a<<2
iii) {a, b}
iv) {2{b}}
v) a ^ b
vi) a|b
vii) a & b
viii) ~ a. **(08 Marks)**

c. Declare following variables in Verilog,
i) A 8-bit vector called a – in
ii) An integer called count. **(02 Marks)**

Module-4

7 a. Discuss sequential and parallel blocks with examples. **(08 Marks)**

b. Write a verilog behavionral description of 8 : 1 multiplexer using case statement. **(06 Marks)**

c. Illustrate the use while loop and repeat loop with examples. **(06 Marks)**

OR

8 a. Explain blocking and non-blocking assignment statements with relevant examples. **(08 Marks)**

b. Write verilog behavioral description of 4-bit binary counter. **(06 Marks)**

c. Write the verilog behavioral description of Dflip – flap. **(06 Marks)**

Module-5

9 a. Define the term logic synthesis. With a neat flow-chart explain computer – Aided logic synthesis process. **(10 Marks)**

b. What will the following statement translate to when run on a logic synthesis tool,
i) assign y = (a&b) | (c&b) where y, a, b, c and d are 3 – bit vectors

ii) if(s)
out = i1 ;
else
out = i0 ; **(10 Marks)**

OR

10 a. With neat flow diagram explain synthesis design flow. **(10 Marks)**

b. Write a notes on :
i) Assign and deassign
ii) Overriding parameters. **(10 Marks)**

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