CBCS SCHEME

USN | | | | | | | | | | |

15EC53

Fifth Semester B.E. Degree Examination, June/July 2023
Verilog HDL

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain a typical design flow for designing VLSI IC circuit using the block diagram. **(06 Marks)**

b. Explain top down design methodology and bottom up design methodology. **(10 Marks)**

OR

2 a. With a block diagram of 4-bit Ripple carry counter, explain the design hierarchy. **(10 Marks)**

b. Explain the trends in Hardware Description Languages (HDLs). **(06 Marks)**

Module-2

3 a. Explain system tasks and compiler directives in verilog. **(06 Marks)**

b. What are the basic components of a module? Explain all the components of a verilog module with a neat block diagram. **(06 Marks)**

c. Write verilog description of SR Latch. Also write stimulus code. **(04 Marks)**

OR

4 a. Write a notes on: i) Registers ii) Nets iii) Arrays iv) Parameters v) Vectors vi) Memories. **(12 Marks)**

b. Declare a top-level module "Stimulus". Define Reg_in (4 bit) and Clk (1 bit) as register variables and Reg_out (4 bits) as wire. Instantiate the module "shift-reg" in "stimulus" block and connect the ports by ordered list. Declare A (4 bit) and clock (1 bit) as inputs and B (4 bit) as output in "shift-reg" module. (No need to show internals). Write a verilog code for the above. **(04 Marks)**

Module-3

5 a. With the help of logic diagram, write a verilog code for 4 to 1 multiplexer using gate – level modeling. **(08 Marks)**

b. What are rise, fall and turn-off delays? Explain, how they are specified in verilog. **(08 Marks)**

OR

6 a. Explain conditional and concatenation operator with an example. **(06 Marks)**

b. Write a verilog dataflow description for 4-bit full adder with carry lookahead. **(10 Marks)**

Module-4

7 a. Explain the blocking assignment statements and non-blocking assignment statements with relevant examples. **(08 Marks)**

b. Write a note on the following loop statements:
i) While loop ii) forever loop. **(08 Marks)**

OR

8 a. Explain sequential and parallel blocks with examples. **(08 Marks)**

b. Write a verilog program for 8-to-1 multiplexer using case statement. **(08 Marks)**

Module-5

9 a. Explain the design tool flow followed in VLSI design with a neat flow diagram. **(10 Marks)**

b. Write VHDL Data flow description of 1 Bit full Adder. **(06 Marks)**

OR

10 a. Explain the relationship between a design entity and its entity declaration and architecture body in VHDL. **(10 Marks)**

b. Write VHDL structural description of 1 Bit Full Adder. **(06 Marks)**

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